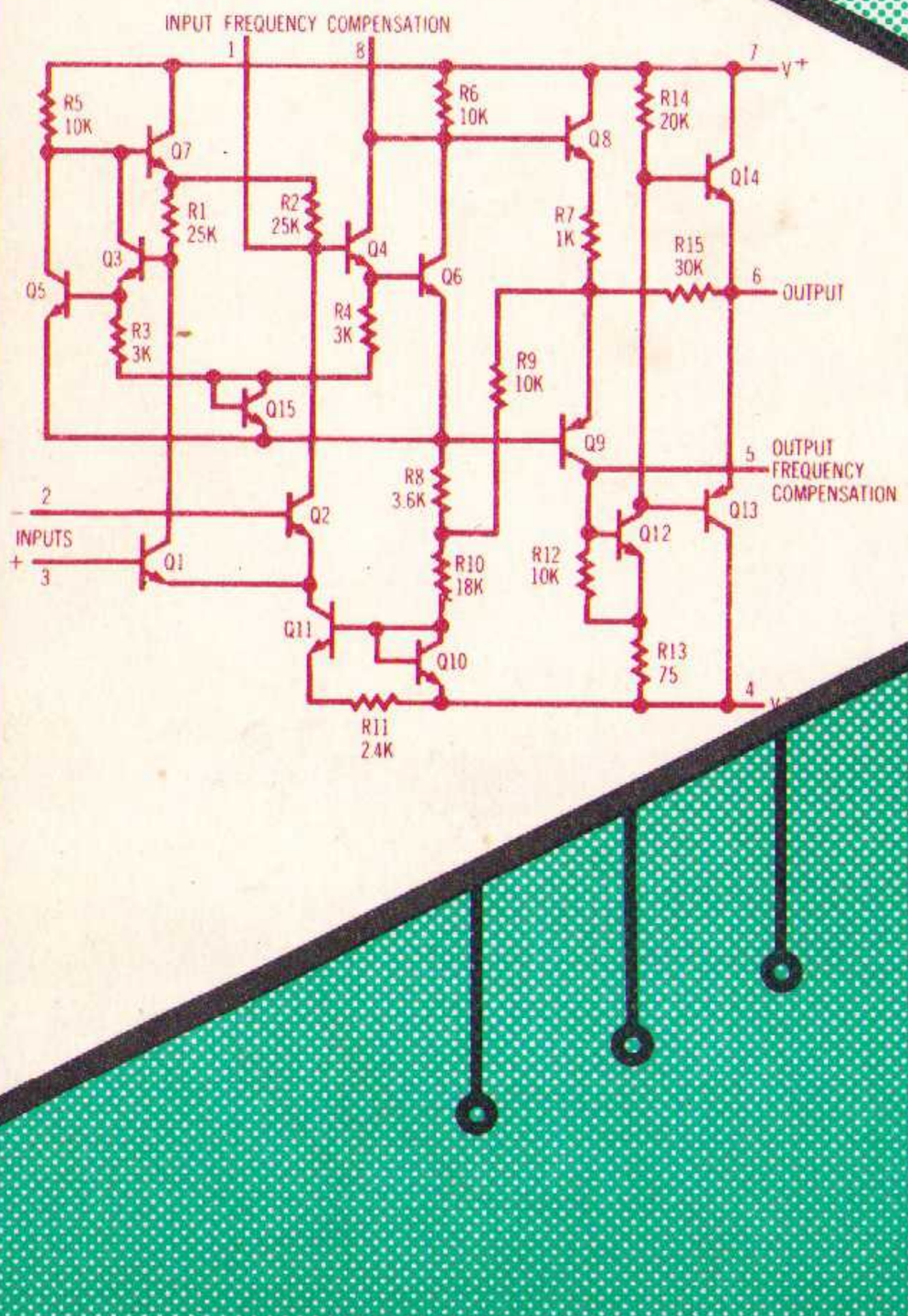
TECHNISCHE DOCUMENTATIE 1970

DEEL 1 2 3 4 5 6 7 8 9 10 11 12

THEORIE EN TOEPASSINGEN VAN DE 709



van dam
ELEKTRONICA

Snellemanstraat 10 - 11 bij Zwaanshals, Rotterdam - noord
Telefoon: 010 - 240812 - 243497, administratie: 010-245516
Giro: 29 55 50. Bankrelatie: Amsterdam-Rotterdam Bank NV.
Postorders en correspondentie: Postbus 3149 te Rotterdam

Filiaal: Blasiusstraat 14-16 bij Ceintuurbaan, Amsterdam
Telefoon: 020-947218.

Prijs: f 5,20

Leveringsvoorwaarden Van Dam Elektronica n.v. - Rotterdam - Amsterdam.

Levering aan particulieren.

Levering aan particulieren vindt uitsluitend à contant, bij vooruitbetaling per giro of per bank, danwel onder rembours plaats. Kortingen worden, gezien onze scherpe prijsnoteringen niet verleend, uitgezonderd bij complete onderdelenpakketten en componenten, waarvoor een staffelprijsnotering geldt. Verzendkosten en -risico zijn ter aller tijde voor rekening koper. Indien één of meerdere artikelen niet in ons leveringsprogramma zijn opgenomen, danwel niet in voorraad zijn, dan zal hiervoor zover mogelijk, een equivalent worden geleverd uit dezelfde prijsklasse. Mocht geen equivalent mogelijk zijn, dan wordt het produkt als niet besteld beschouwd en niet nageleverd. Mocht het betrokken produkt deel uitmaken van een door ons aangeboden onderdelenpakket, dan zal dit produkt wèl worden nageleverd tenzij uitdrukkelijk anders overeengekomen, teneinde te voorkomen, dat een produkt wordt gebruikt, waarvan de kwaliteit de goede werking en algemene kwaliteit van ons ontwerp aantast. Indien dit produkt bij aanschaf van het onderdelenpakket wordt betaald, vindt franco nazending plaats, waarbij de verzendkosten tot maximaal *f* 1,00 voor onze rekening komen. Verpakking wordt niet door ons berekend!

Levering aan industriële afnemers.

Levering aan industriële afnemers uitsluitend à contant of onder rembours, behoudens relaties, welke reeds op rekening geleverd kregen, danwel na bankinformatie. Wij behouden ons het recht voor, levering op rekening te weigeren. Bij levering à contant of onder rembours zullen wij, indien vóóraf kenbaar gemaakt, de B.T.W. apart specificeren; dit gebeurt automatisch bij levering op rekening.
De administratiekosten bij levering op rekening voor orders tot *f* 100,- bedragen in alle gevallen *f* 4,00 per keer; bij levering à contant of onder rembours worden géén administratiekosten in rekening gebracht. Opdrachten boven *f* 50,- worden franco verzonden bij levering op rekening; bij levering onder rembours worden de volledige portokosten berekend. De betalingstermijn is strikt 30 dagen netto na faktuurdatum. Indien binnen 45 dagen geen remise is ontvangen wordt alleen nog à contant of onder rembours geleverd. Zie verder onder "levering aan particulieren".

Levering aan overheidsinstellingen en scholen.

Levering aan overheidsinstellingen en scholen uitsluitend à contant of onder rembours, tenzij uitdrukkelijk anders is overeengekomen (zie ook R.I.B.-handleiding). Bij opdrachten boven *f* 1.000,- wordt een korting verleend van 10%, tenzij reeds van een staffelprijs of andere korting gebruik gemaakt wordt. Administratiekosten voor orders beneden *f* 100,- bedragen *f* 4,00/order. Opdrachten boven *f* 50,- worden franco verzonden. Zie ook "levering aan particulieren en industriële afnemers".

Levering aan detaillisten: als overheidsinstellingen en scholen, tenzij anders wor overeengekomen.

Prijsnoteringen en levertijden.

Alle door ons afgegeven prijsnoteringen zijn incl. BTW, tenzij uitdrukkelijk anders is aangegeven. Deze prijzen kunnen door stijging van produktiekosten, materiaalprijzen en koersverschillen aan verandering onderhevig zijn; wij behouden ons het recht voor deze door te berekenen. Voor de netto- of "BTW-schone" prijs geldt bij 12% B.T.W. een vermenigvuldig faktor van 0,8929. In het algemeen is de levertijd uit voorraad Rotterdam; wij stellen ons niet aansprakelijk voor het tijdelijk ontbreken van een of meerdere produkten i.v.m. de internationale leversituatie en gevallen van overmacht. Orders, welke niet uit voorraad geleverd kunnen worden en door ons schriftelijk bevestigd worden, kunnen niet worden geanuleerd.

Slotopmerkingen.

Wij behouden ons het recht voor wijzigingen in ons leveringsprogramma aan te brengen. Tevens stellen wij ons niet aansprakelijk voor het ontbreken van een of meerdere produkten, het uitvallen resp. niet goed functioneren van apparatuur/onderdelen en de eventueel daardoor ontstane schade.

LEVERING OP REKENING OF ONDER REMBOURS UITSLUITEND VIA ONS BEDRIJF TE ROTTERDAM-NOORD.
RICHT UW ORDERS UITSLUITEND AAN: Van Dam Elektronica, Afd. Verkoop, Postbus 3149 te Rotterdam. Telefonische orders: 010-240812-243497. Administratie: 010-245516.

Abonnementen.

Op deze uitgave, welke inmiddels zijn derde jaargang is ingegaan, is een jaarabonnement mogelijk bij vooruitbetaling van *f* 10,40/jaar incl. 4% B.T.W. op onze postgirorekening 295550 t.n.v. Van Dam N.V., Postbus 3149 te Rotterdam-noord. Abonnementen gaan in per 1 januari en eindigen op 31 december van hetzelfde jaar. Eventuele bijvoegsels van fabrikanten, danwel van Van Dam Elektronica, vallen niet onder dit abonnement en worden gratis verstrekt.

Verhuizingen van abonné's.

Elke abonné is in ons adresseersysteem ondergebracht onder een op de enveloppe vermeld administratienummer. Bij verhuizing, adrescorrectie of correspondentie over Uw abonnement dient beslist dit nummer te worden vermeld. Correspondentie dient U uitsluitend te richten aan: Van Dam Elektronica, Afd. TD 1970, Postbus 3149 te Rotterdam.

Doelstelling.

Het doel van deze uitgave "Technische Documentatie" is het op de hoogte houden van geinteresseerde amateurs en technici van recente technologische en technische ontwikkelingen op het gebied van de elektronica bij fabrikanten met een internationale bekendheid, alsmede van de toepassingen van deze moderne produkten.

Middelen.

Om het voornoemde doel te bereiken wordt jaarlijks 250-300 pagina's technische informatie verstrekt, welke de volledige datasheets, meetschakelingen en eventuele toepassingen van nieuwe ontwikkelingen omvatten. Deze informatie wordt ons verstrekt door de betrokken fabrikanten resp. hun vertegenwoordigingen en wordt door ons in onverkorte en onvertaalde vorm gecoördineerd tot een waardevolle informatie. Tevens worden toepassingen, welke door onze research-afdeling ontwikkeld zijn, in deze documentatie opgenomen.

Verschijningsdata.

Deze uitgave bestaat uit 12 delen à minimaal 20 pagina's, waarbij wij het recht voorbehouden, indien de binnengekomen documentatie danwel het besproken onderwerp dit wenselijk maken, één of meerdere delen te combineren; deze uitgave kan derhalve niet de pretentie 'maandblad' meekrijgen.

Technische documentatie 1970 Deel 1, 2, 3 en 4.

Jaarabonnement: ƒ 10,40 bij vooruitbetaling op giro 295550 t.n.v. Van Dam Elektronica, Postbus 3149 te Rotterdam-noord onder vermelding van : t.b.v. TD 1970.

- -

Inleiding. Coördinatie: Paul E. Annokkee

Deze eerste uitgave in 1970 vormt een combinatie van de delen 1 t/m 4. Wij hebben deze combinering wenselijk geacht in verband met het besproken onderwerp, de operationele versterker type 709.

Deze geïntegreerde schakeling biedt een enorm aantal mogelijkheden, waaruit voor deze documentatie een byzonder ruime keuze gemaakt is. Deze documentatie is tot stand gekomen met internationale medewerking van de volgende fabrikanten en publiciteitsmedia:

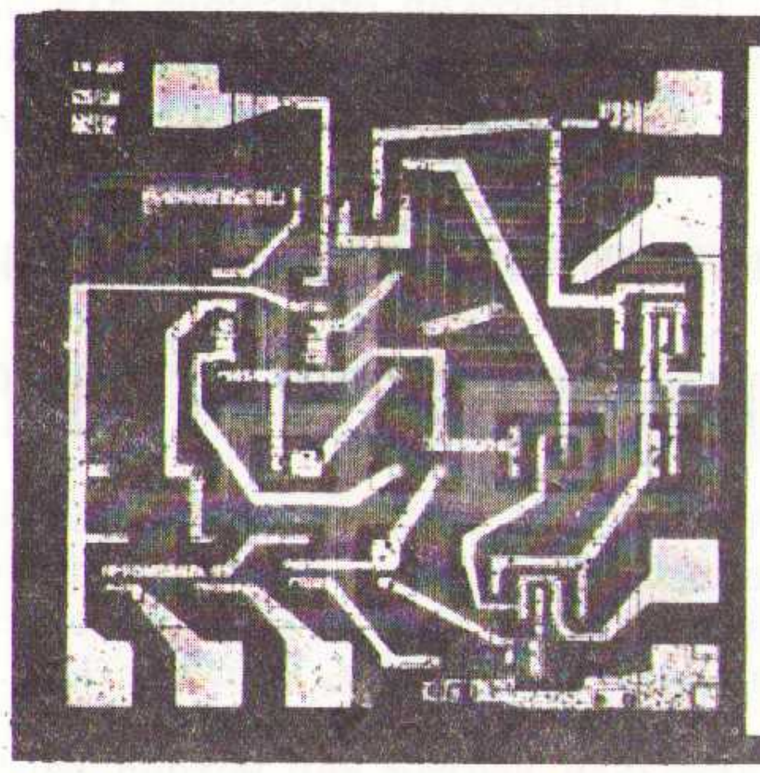
SGS, Texas Instuments Incorporated, Signetics, Motorola Incorporated, National Semicondustor Corporation, Fairchild, Transitron en Electronic Design.

Wij danken deze fabrikanten en hun nederlandse vertegenwoordigers voor de verleende medewerking.

Mochten er in de loop van dit jaar nog meer toepassingen binnenkomen van fabrikanten, danwel abonné's, dan zullen wij ook deze opnemen.

Waarom de 709 zo uitgebreid behandeld wordt? Deze geïntegreerde schakeling heeft in zijn vele bestaansjaren bewezen niet alleen voor "supertechnici" geschikt te zijn, doch een groot toepassingsgebied aan het licht gebracht. Zo kan deze schakeling worden gebruikt bij de constructie van audio-versterkers, voedingen, A/D converters, D/A converters, oscillatoren, meetinstrumenten, meetversterkers, filterschakelingen, differentiaal schakelaars, logarithmische versterkers, zaagtand-generatoren, vermenigvuldig- en deel-schakelingen, servo-sturingen, enz., enz.

Daarnaast is de stuksprijs van deze operationele versterker op een dusdanig niveau gekomen, dat toepassing op grotere schaal ook hierdoor wordt gerechtvaardigd.



Wij hopen met deze uitgebreide documentatie van de operationele versterker 709 te hebben bijgedragen tot vele leerzame en interessante experimenten, welke zullen leiden tot een groter toepassingsgebied voor deze en de vele andere geïntegreerde schakelingen.

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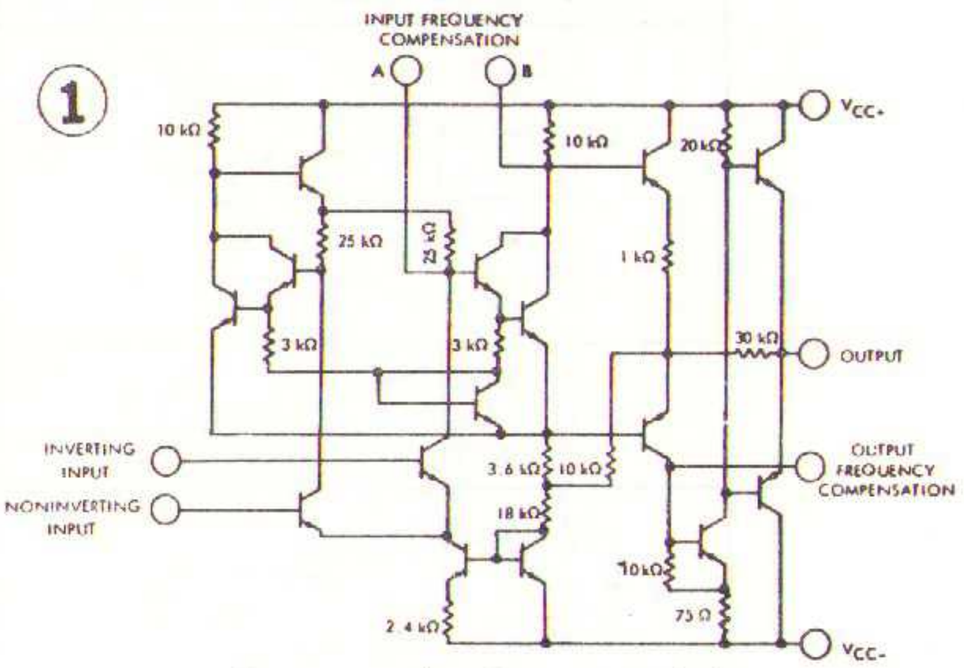
709 OP-AMP

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift — ±3 μV/°C
- Large Output Voltage Swing —
  ±14 V typical @ ±15 V Supply
- Low Output Impedance — Z_{out} = 150 ohms typical

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

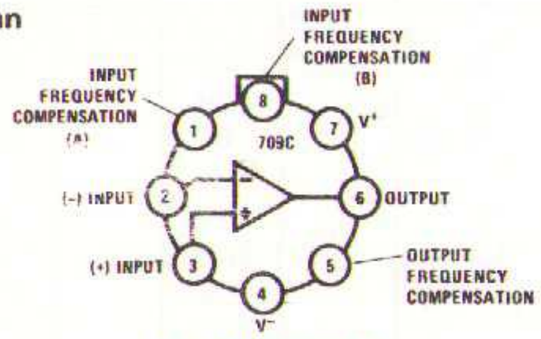
Rating	Symbol	Value	Unit
Power Supply Voltage	V^+ V^-	+18 -18	Vdc Vdc
Differential Input Signal	V_{in}	±5.0	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above 25°C Flat Package Derate above 25°C Plastic Package Derate above 25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range*	T_A	0 to +75	°C
Storage Temperature Range Metal Can and Flat Package Plastic Package	T_{stg}	 -65 to +150 -65 to +125	°C



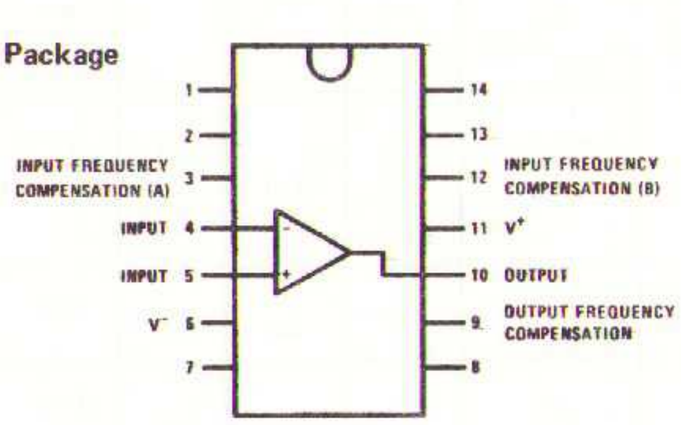
Component values shown are nominal.

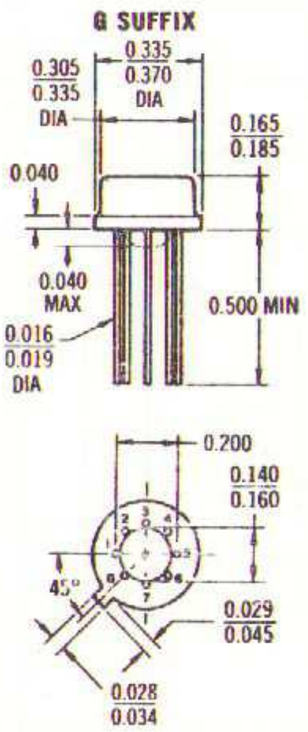
SCHEMATIC DIAGRAM

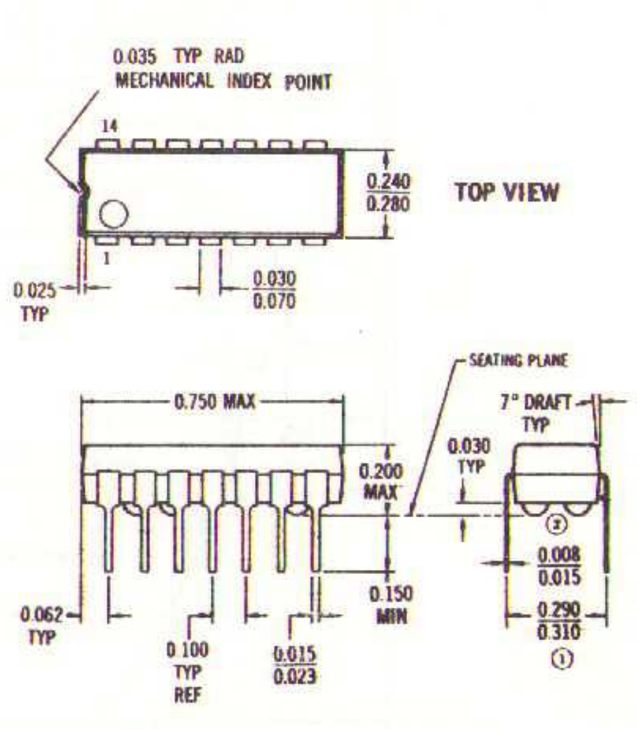
Metal Can



Dip Package







PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H
"G" Package	1	2	3	4	5	6	7	8
"F" Package	2	3	4	5	6	7	8	9
"P" Package	3	4	5	6*	9	10	11	12

*Pin 7 is electrically connected to substrate and V^-

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 1 — TEST CIRCUIT
V^+ = +15 Vdc, V^- = −15 Vdc, T_A = 25°C

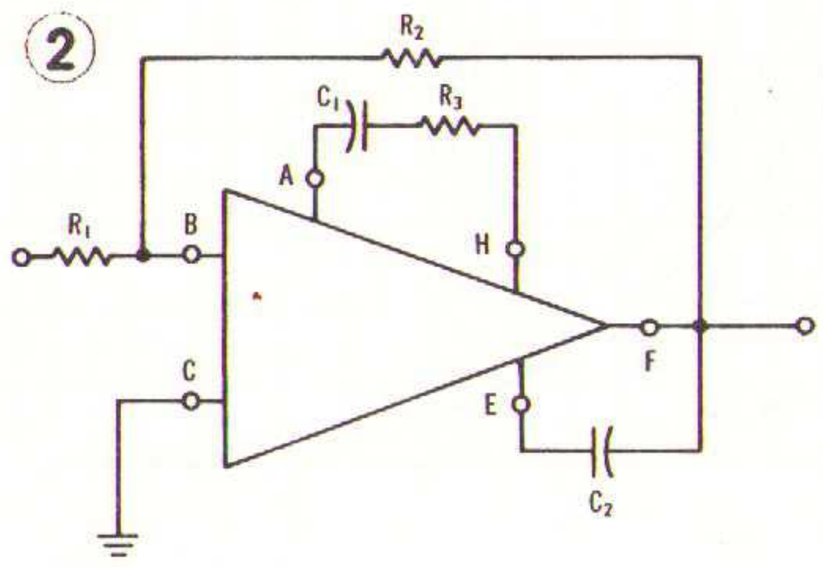
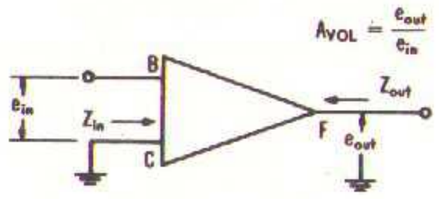
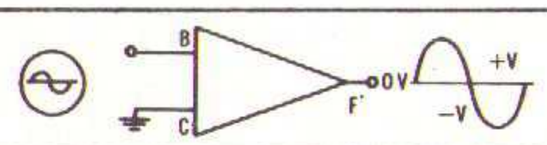
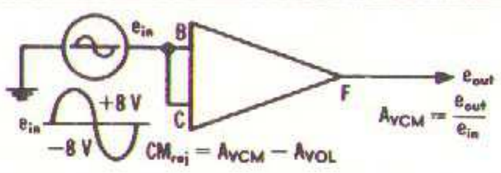
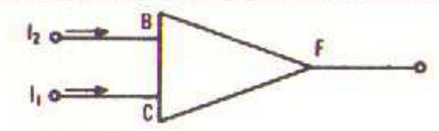
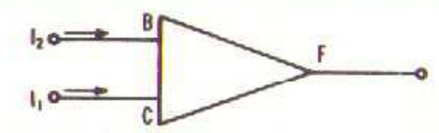
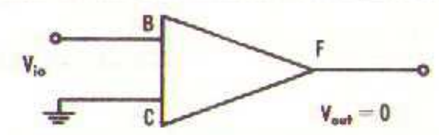
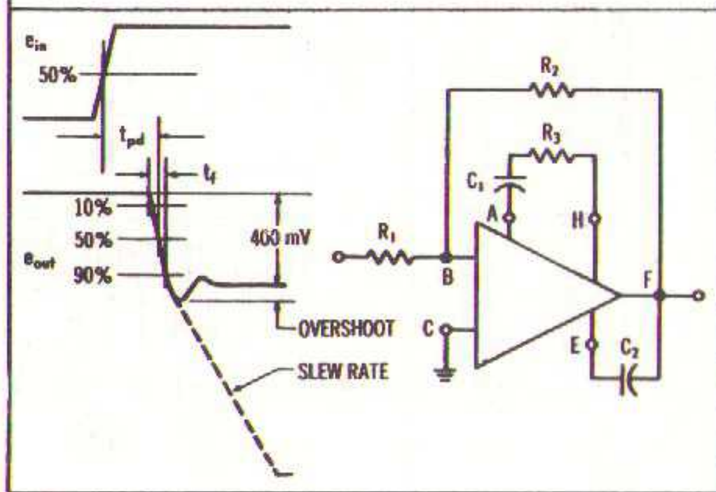
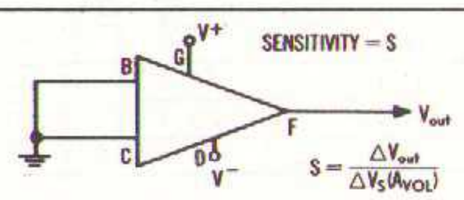


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (pF)	C_2 (pF)
2	1	10 k	10 k	1.5 k	5 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1M	1.5 k	100	3
	4	1 k	1M	0.	10	3
3	1	1 k	1M	0	10	3
	2	10 k	1M	1.5 k	100	3
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5 k	200
4	1	0	∞	1.5 k	5 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3
	4	0	∞	0	10	3

ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = 25°C$ unless otherwise noted)

Characteristic Definitions (linear operation)	Characteristic	Symbol	Min	Typ	Max	Unit
	Open Loop Voltage Gain (R_L=2 kΩ, V_{out} = ± 10 V, T_A = 0°C to +75°C)	A_{VOL}	15,000	45,000	-	-
	Output Impedance (f = 20 Hz)	Z_{out}	-	150	-	Ω
	Input Impedance (f = 20 Hz)	Z_{in}	50	250	-	kΩ
	Output Voltage Swing (R_L = 10 kΩ) (R_L = 2 kΩ)	V_{out}	±12 ±10	±14 ±13	- -	V_{peak}
	Input Common Mode Voltage Swing	CMV_{in}	±8.0	±10	- -	V_{peak}
	Common Mode Rejection Ratio	CM_{rej}	65	90	-	dB
	Input Bias Current $\left(I_b = \frac{I_1 + I_2}{2}\right)$, ($T_A$ = +25°C) (T_A = 0°C)	I_b	- -	0.3 -	1.5 2.0	µA
	Input Offset Current ($I_{io} = I_1 - I_2$) ($I_{io} = I_1 - I_2$, T_A = 0°C) ($I_{io} = I_1 - I_2$, T_A = +75°C)	I_{io}	- - -	0.1 - -	0.5 0.75 0.75	µA
	Input Offset Voltage (T_A = 25°C) (T_A = 0°C, +75°C)	V_{io}	- -	2.0 -	7.5 10	mV
	Step Response {Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3 pF} {Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF} {Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF}	t_f t_{pd} dV_{out}/dt ① t_f t_{pd} dV_{out}/dt ① t_f t_{pd} dV_{out}/dt ①	- - - - - - - - -	0.8 0.38 12 0.6 0.34 1.7 2.2 1.3 0.25	- - - - - - - - -	µs µs V/µs µs µs V/µs µs µs V/µs
	Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = 0°C to +75°C) ($R_S \leq$ 10 kΩ, T_A = 0°C to +75°C)	TC_{Vio}	- -	3.0 6.0	- -	µV/°C
	DC Power Dissipation (Power Supply = ±15 V, V_{out} = 0)	P_D	-	80	200	mW
	Positive Supply Sensitivity (V^- constant)	S^+	-	25	200	µV/V
	Negative Supply Sensitivity (V^+ constant)	S^-	-	25	200	µV/V

① dV_{out}/dt = Slew Rate

FIGURE 2 — LARGE SIGNAL SWING versus FREQUENCY

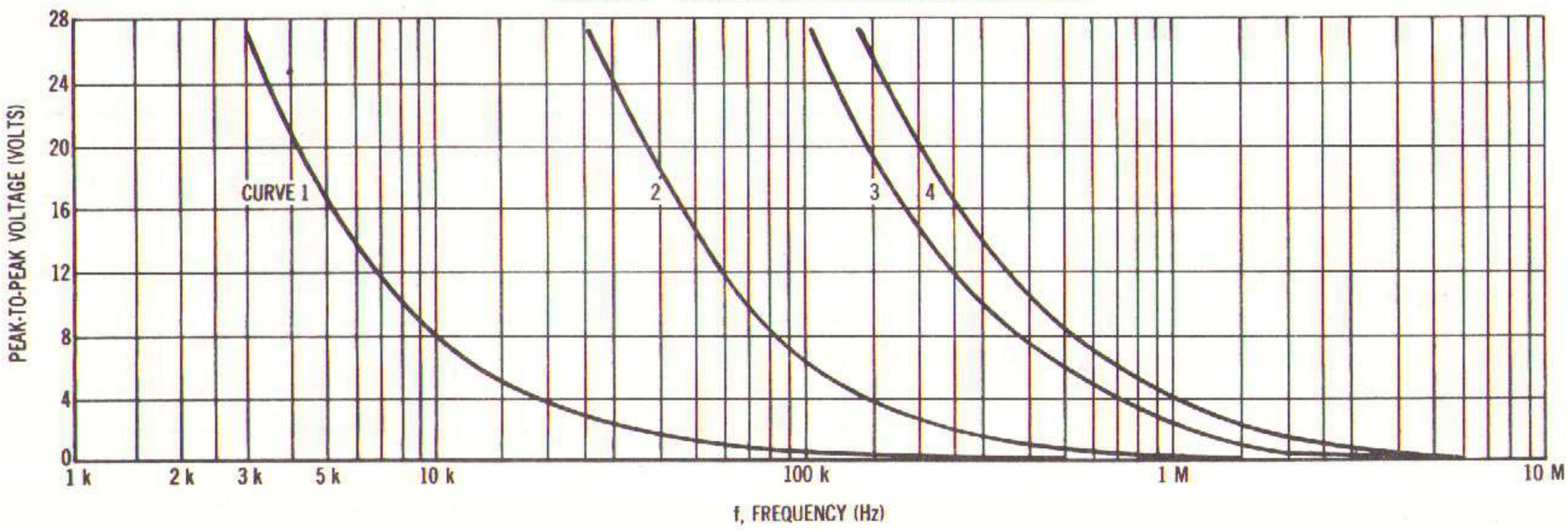


FIGURE 3 — VOLTAGE GAIN versus FREQUENCY

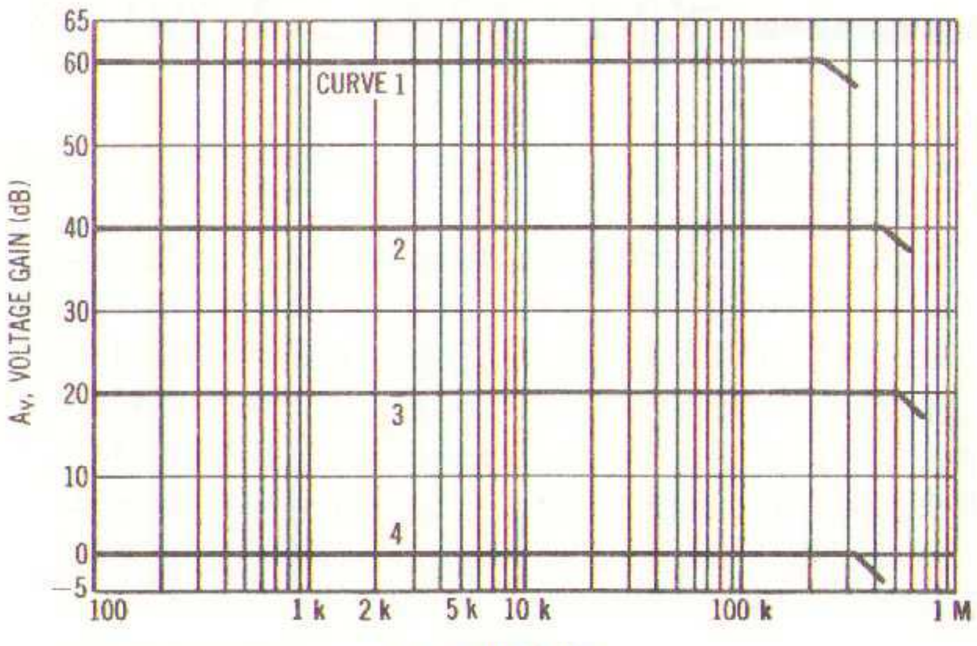


FIGURE 4 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

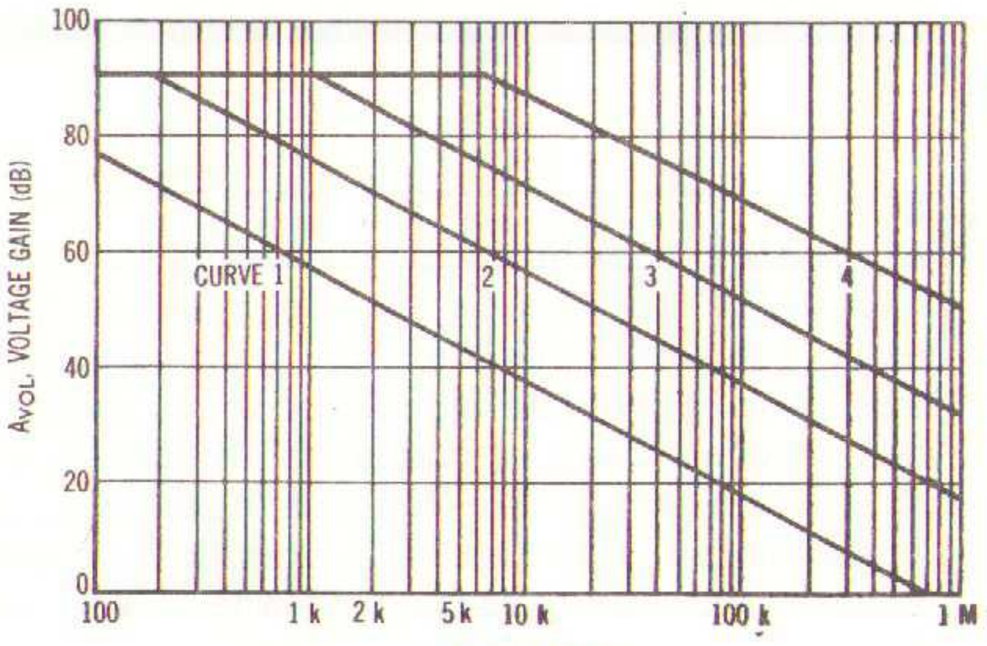


FIGURE 5 — POWER DISSIPATION versus POWER SUPPLY VOLTAGE

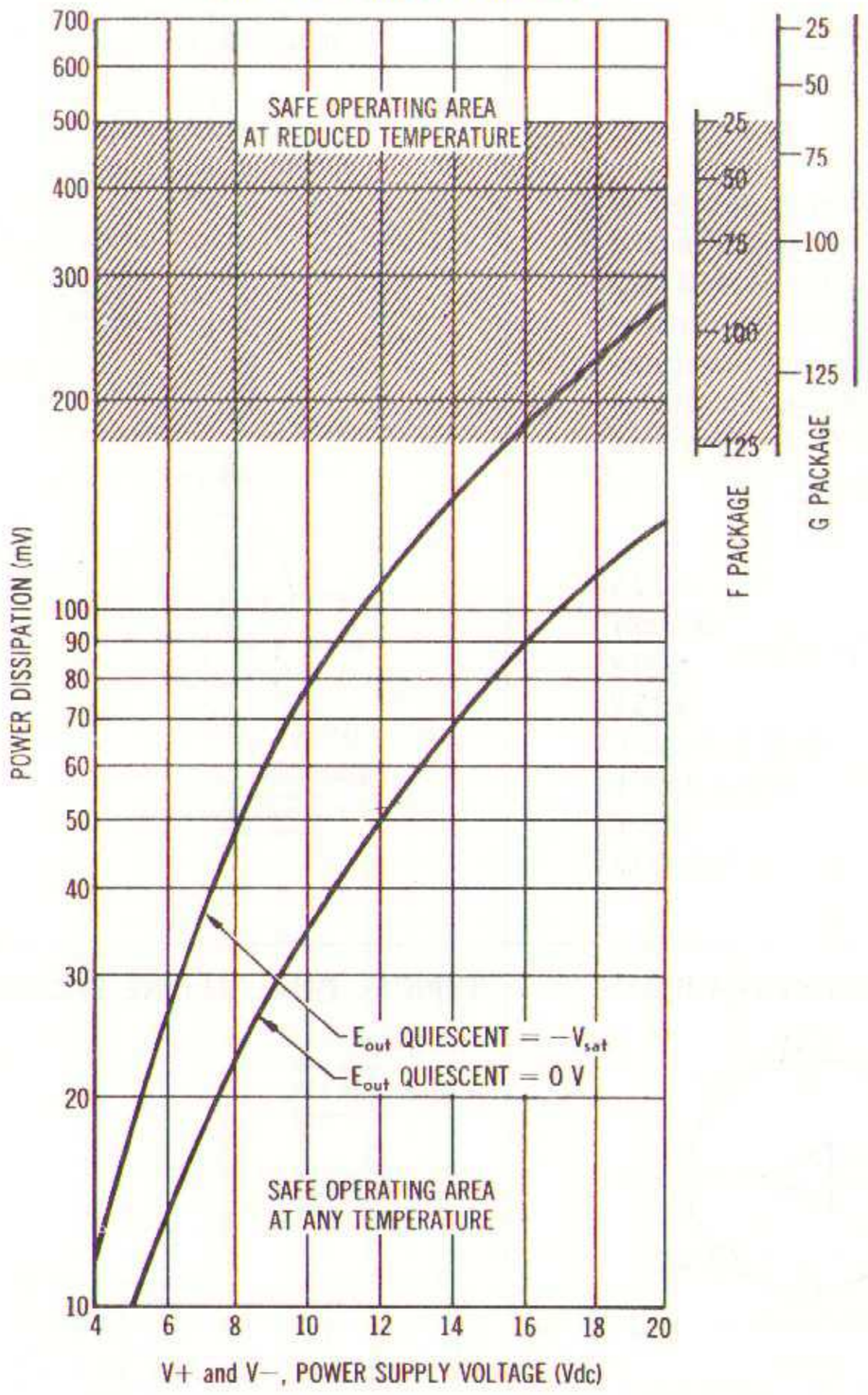


FIGURE 6 — VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

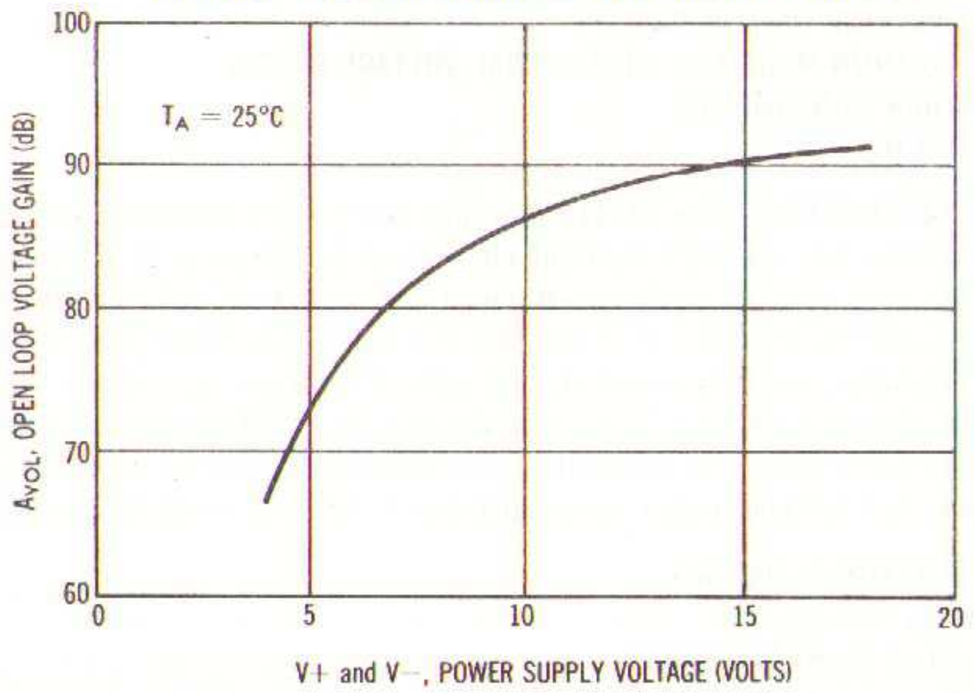


FIGURE 7 – OUTPUT SWING versus POWER SUPPLY VOLTAGE

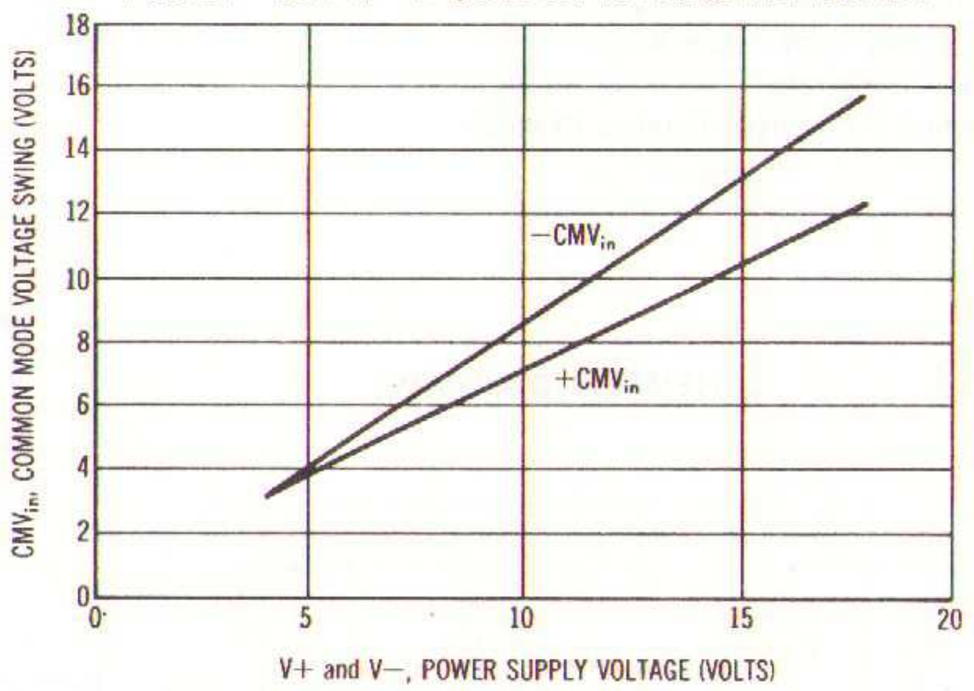


FIGURE 8 — INPUT OFFSET VOLTAGE versus TEMPERATURE

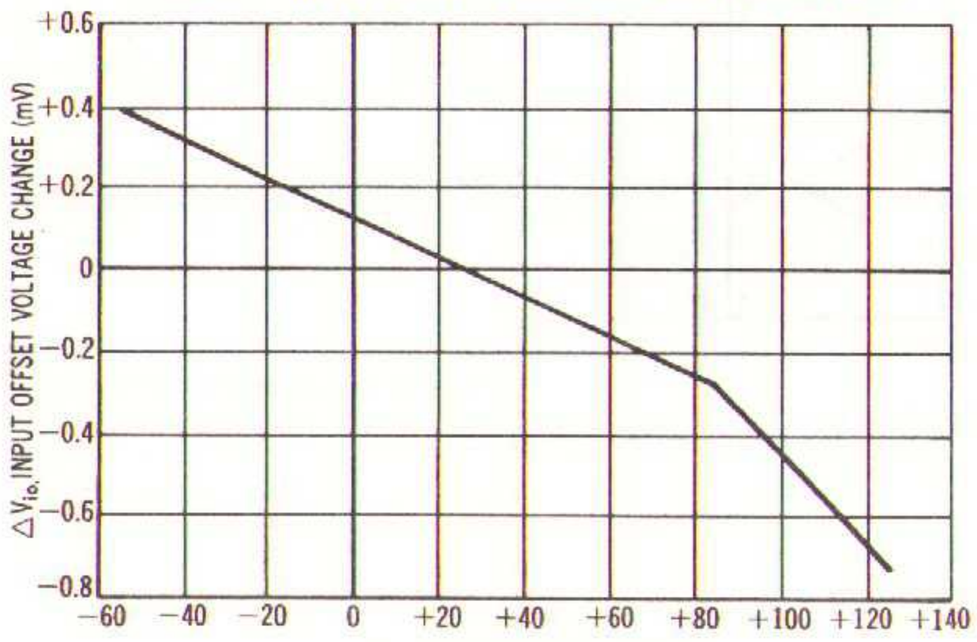
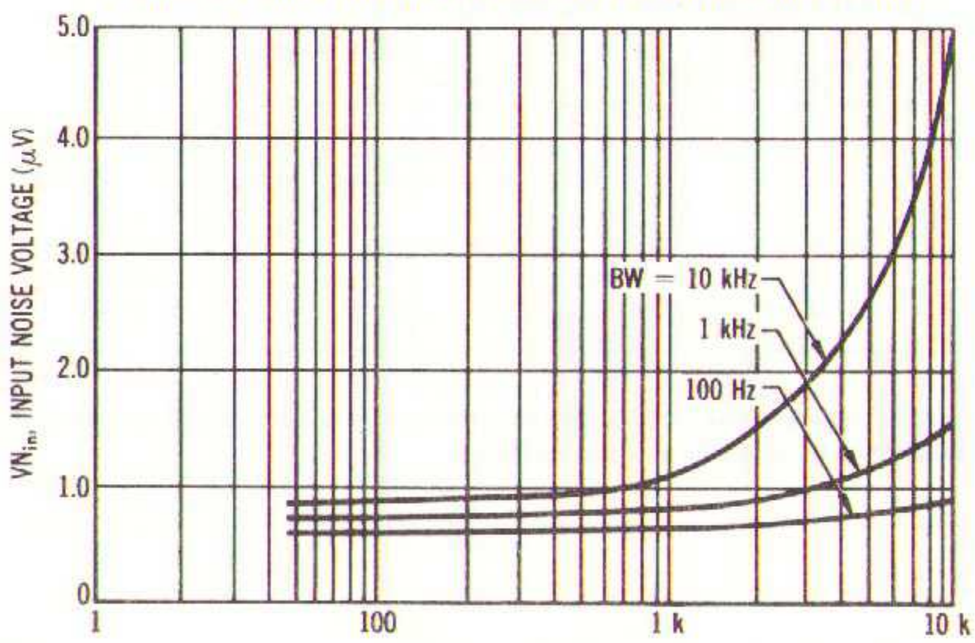


FIGURE 9 — INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



741 OP-AMP

Verscheidene fabrikanten hebben een nieuw type operationele versterker ontwikkeld welke in plaats van de bekende 709 kan worden gebruikt. Dit type is op de markt gebracht als de 741, waarvan hieronder het datasheet is opgenomen. Bij deze geïntegreerde schakeling is géén frequentie-compensatie meer nodig, terwijl tevens twee extra aansluitingen aangebracht zijn voor compensatie van de offset-spanning. De 741 kan ook in alle in deze documentatie opgenomen toepassingsvoorbeelden worden gebruikt na aanpassing van de betrokken schakeling ten aanzien van de eerder genoemde compensaties.

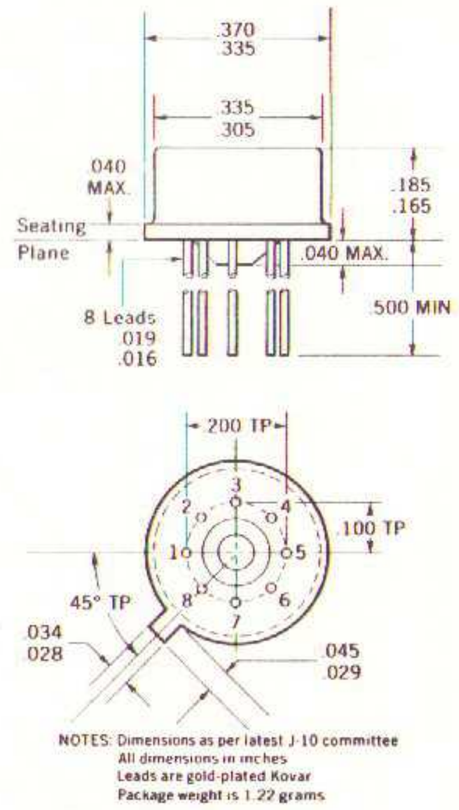
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA741C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741C is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (−55°C to +125°C) see μA741 data sheet.

ABSOLUTE MAXIMUM RATINGS

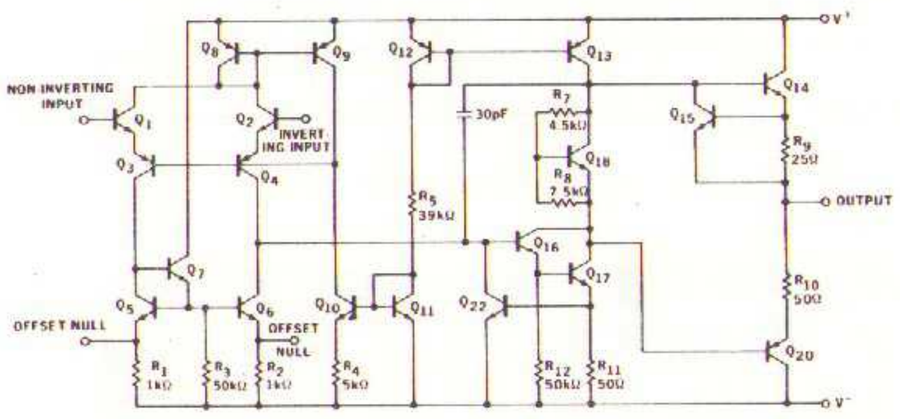
Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 2)	Indefinite

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline

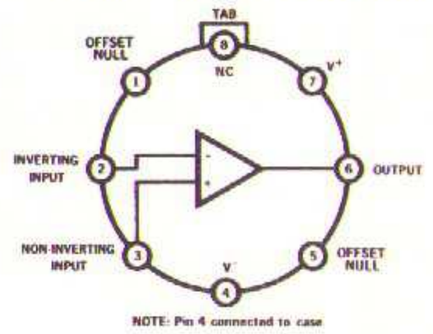


NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

3 SCHEMATIC DIAGRAM

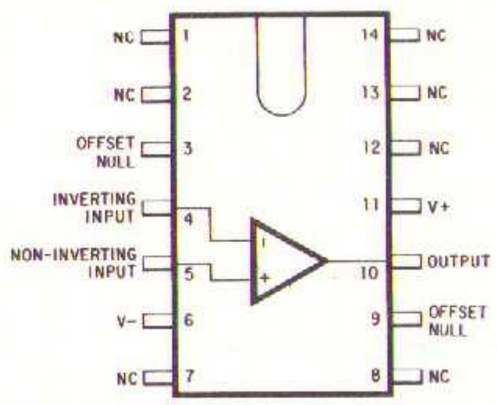


CONNECTION DIAGRAMS

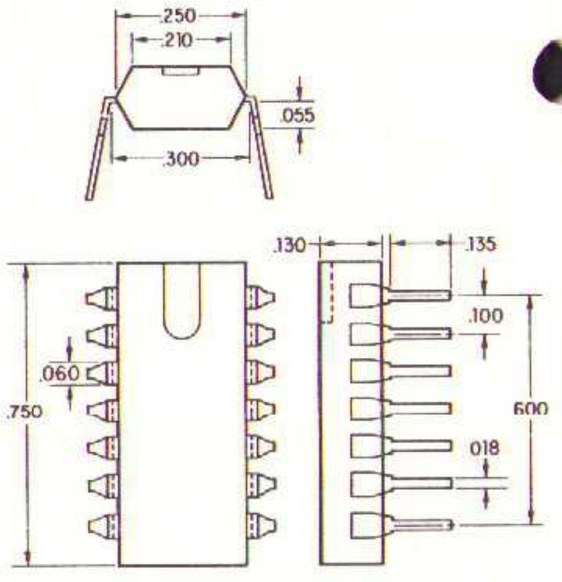


NOTE: Pin 4 connected to case

(TOP VIEW)



TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

NOTES:
(1) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(2) Short circuit may be to ground or either supply.

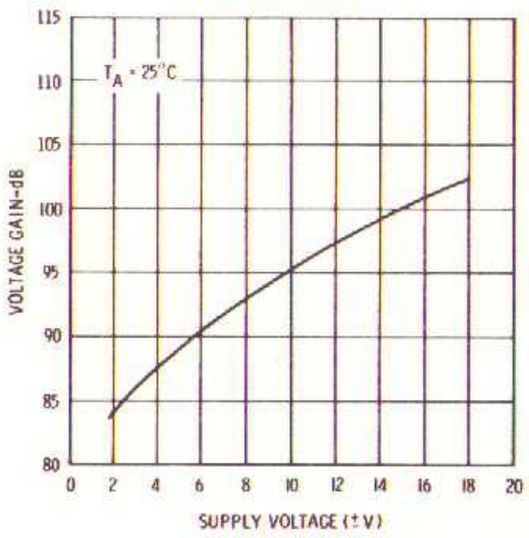
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified) Read = 741 L

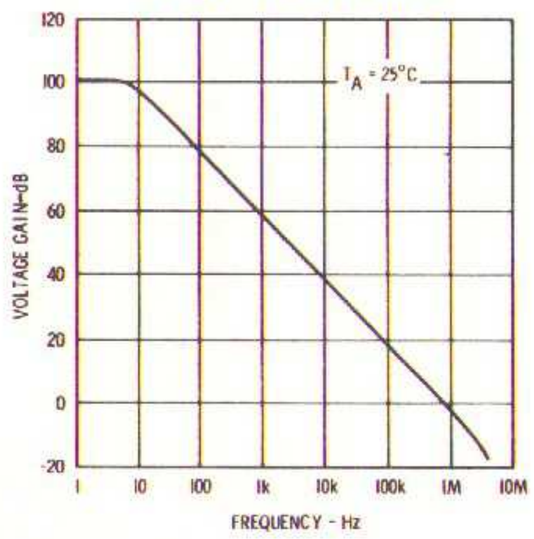
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0	5 MΩ.	MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	100,000 2.10^5		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

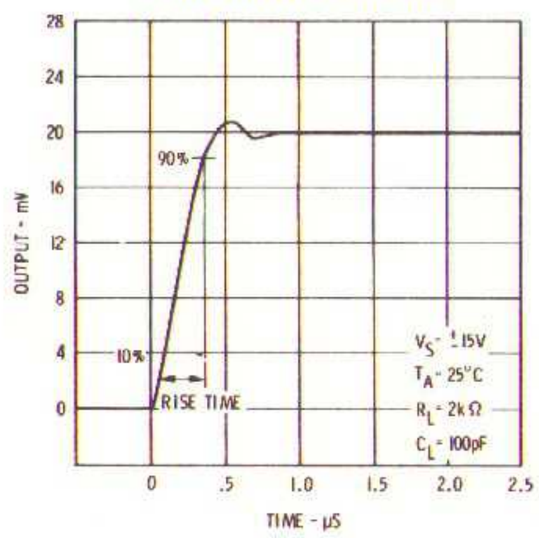
OPEN LOOP VOLTAGE GAIN



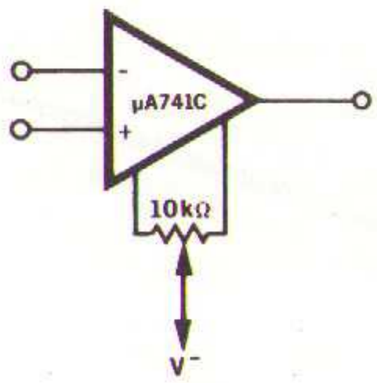
OPEN LOOP FREQUENCY RESPONSE



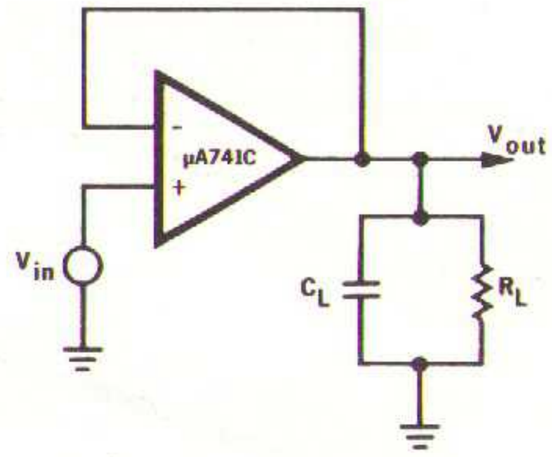
TRANSIENT RESPONSE



4 **VOLTAGE OFFSET NULL CIRCUIT**



5 **TRANSIENT RESPONSE TEST CIRCUIT**



A A N T E K E N I N G E N

N O T E S

THEORY

2.5 DESCRIPTION OF 709 CIRCUIT OPERATION

2.5.1 Introduction

The 709 is a high-gain operational amplifier intended for use in D.C. servo systems and high impedance analogue computers, also for low-level instrumentation applications and for the generation of special linear and non-linear functions.

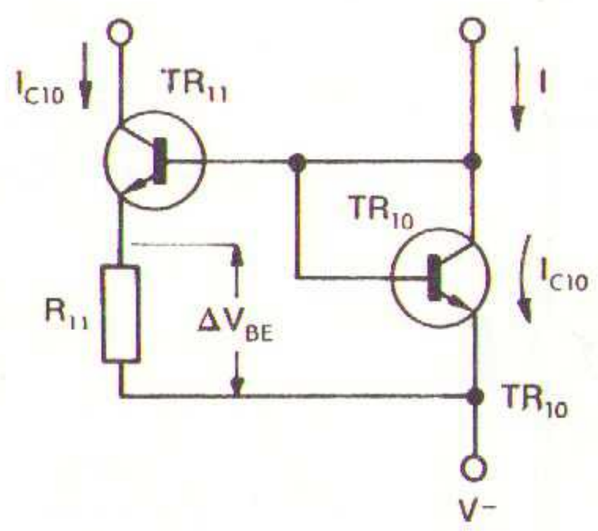
The circuit described below has been designed employing the basic philosophies outlined in Section 2.1. It gives a performance which is comparable to the best discrete component designs, yet it is relatively simple to build in monolithic form. It features low offset, high input impedance, a large input common mode range, high gain, low power consumption and a large output swing under load. The amplifier displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The suitability of the circuit for integration is indicated by the fact that it is constructed on a 0.035 mm^2 silicon die using a six-mask Planar epitaxial process which is nearly indentical to that employed with common digital integrated circuits.

2.5.2 Input Stage

Darlington-input amplifiers have generally been used in microcircuits requiring high input impedance because of restrictions on maximum resistance values, which make it difficult to operate transistors at low collector currents. With D.C. amplifiers, the Darlington connection has the disadvantage of considerably higher offset and thermal sensitivity than a non-Darlington differential pair. In addition, input impedance and input currents vary as the square of the current gain with a Darlington connection, so it does not provide a great performance advantage when full temperature range operation is considered. The described design is a departure from this conventional approach: the input stage is operated at low collector currents but without requiring usually large resistance values.

One unusual feature of the input stage is the current source for the emitters of the input transistors which is shown in Fig. 2.29.

It makes use of the highly predictable difference



$$\Delta V_{BE} = V_{BE10} - V_{BE11}$$

$$= \frac{KT}{q} \log_e \frac{I_{C10}}{I_{C11}}$$

$$I_{C11} \cong \frac{\Delta V_{BE}}{R_{11}}$$

Fig. 2.29 - Simplified Circuit of Input Stage Current Source

in the emitter-base voltage of two identical transistors operating at different collector currents to form a microampere current source using resistances of only a few kilohms.

With reference to Fig. 2.29, a relatively-large current (I) is passed through the diode-connected transistor, TR_{10}. Assuming large current gains for TR_{10} and TR_{11}, the collector current of TR_{10} will be equal to this current. The emitter-base voltage of TR_{10} is used to bias the current source, TR_{11}. The resistor in the emitter of TR_{11} determines the collector current of the device.

This type of current source is described in detail in Section 2.1.2; but to give an example of its operation, it might be assumed that the biasing transistor TR_{10} is operating at 1 mA collector current and that it is desired to operate TR_{11} at 10 μA. For this ratio of collector currents, the emitter-base voltage difference between the two devices will be 120 mV at room temperature (60 mV/decade). Therefore, it is only necessary to insert a 12 kΩ resistor in the emitter of TR_{11} to obtain the desired 10 μA collector current.

The differential input stage (TR_1 and TR_2) and its collector load resistors (R_1 and R_2) are shown in the complete circuit of Fig. 2.32. The input stage operates at approximately 20 μA collector current. The collector load resistors are relatively small for this current level, but they do provide enough gain to make the effect of second stage offset small if the second stage is reasonably well balanced.

Another interesting feature of this input stage is that the variation in current-source current with temperature almost exactly compensates for the variation in input stage transconductance. As a result, the voltage gain holds constant, within a few percent, over the full operating temperature range of the circuit. In addition, the collector current of the current source is roughly proportional to the logarithm of the collector current of its biasing transistor. Since the collector current of the biasing transistor varies approximately as the supply voltage, the input stage operating level is practically unaffected by supply voltage changes.

2.5.3 Second Stage

The second stage design is similar to that described in Section 2.1.2. A simplified circuit is shown in Fig. 2.30.

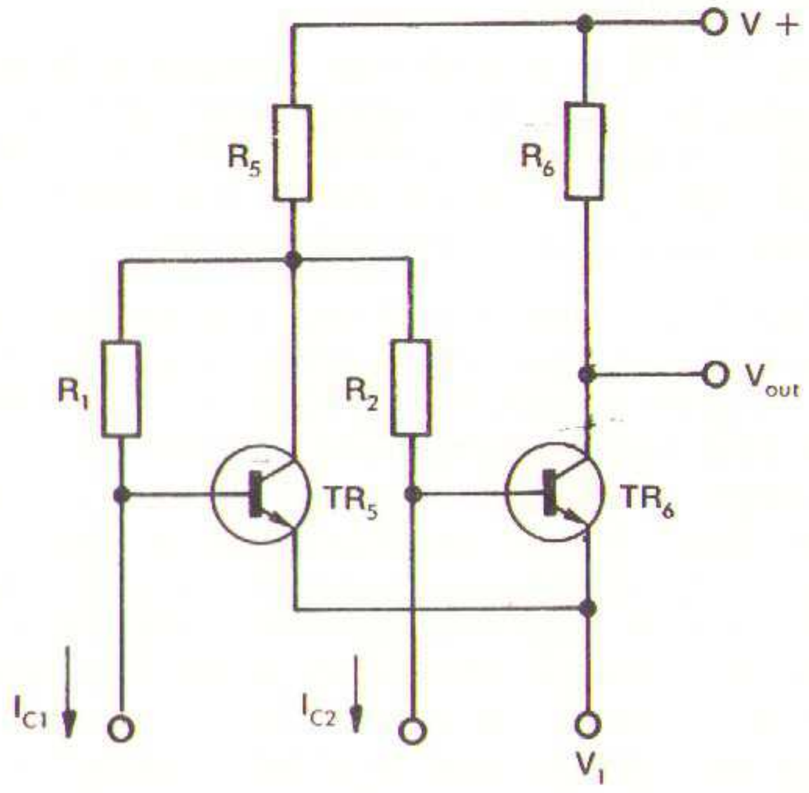
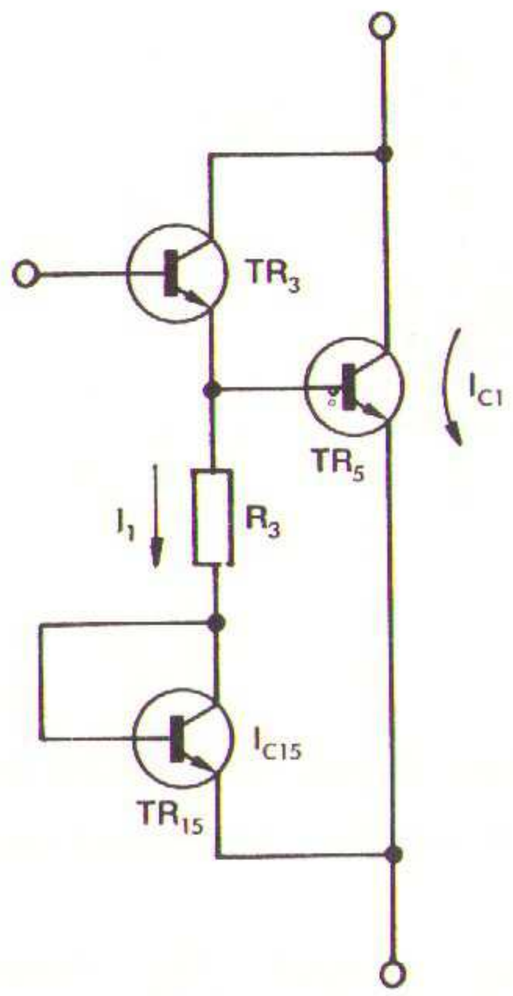


Fig. 2.30 - Simplified Circuit of Second Stage



$$\Delta V_{BE} = V_{BE5} - V_{BE15}$$

$$= \frac{KT}{q} \log_e \frac{I_{C5}}{I_{C15}}$$

$$I_1 = \frac{\Delta V_{BE}}{R_1}$$

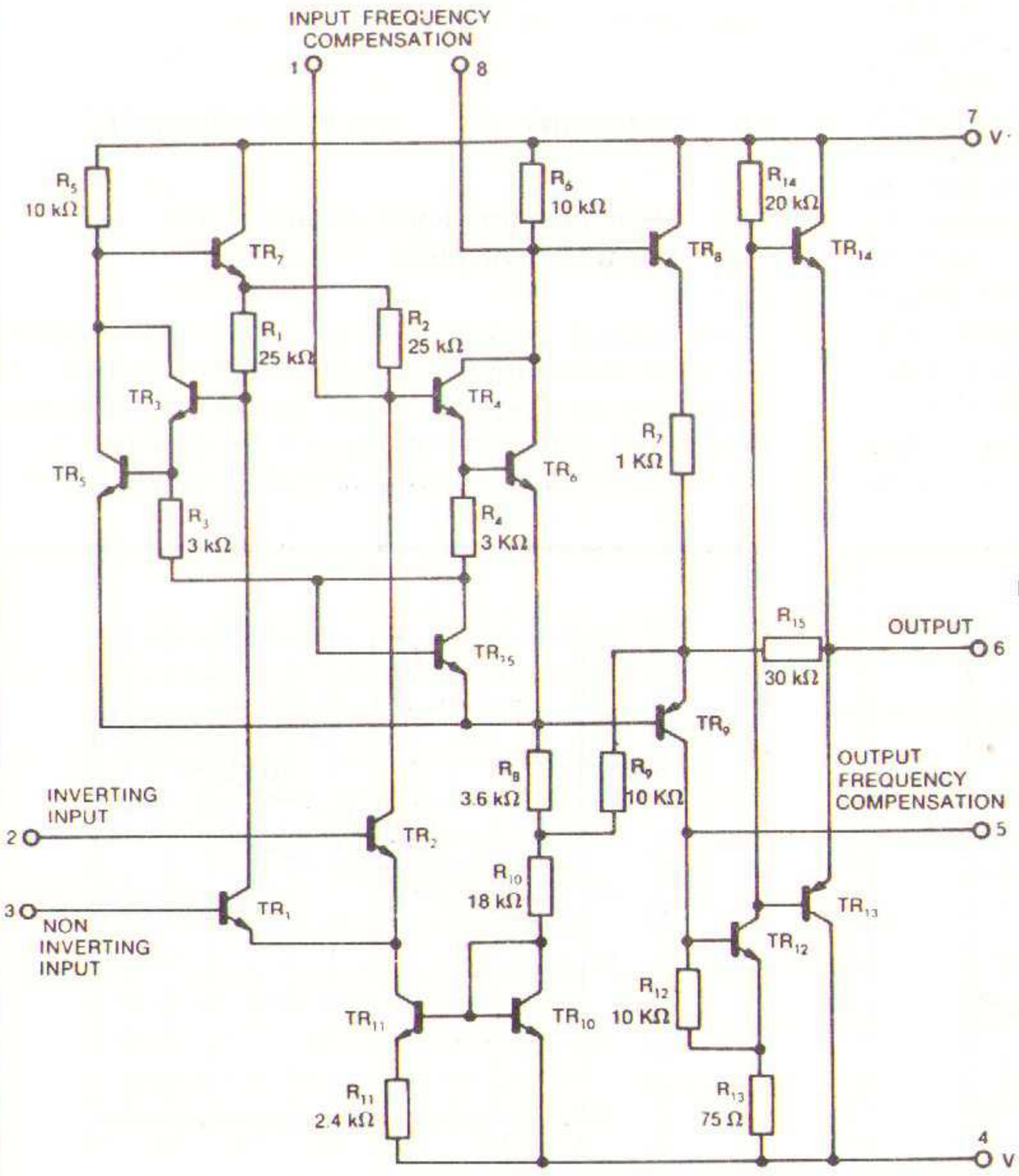
Fig. 2.31 - Circuit Illustrating Principle of the Modified Darlington Connection

The input stage collectors are connected to the bases of the second stage transistors. The collector load resistors of the input stage, R_1 and R_2, are connected as shown. In the simplified circuit, TR_6 is the second stage amplifier while TR_5 provides balanced biasing. TR_5 also serves as a unity gain inverter, delivering the full differential output of the input stage to the base of TR_6. This helps to minimise offset and thermal drift since the input stage has low gain because of the low-value collector load resistors. As pointed out in Section 2.1.2, this second stage design is extremely useful in going from a differential to a single-ended connection in that it provides excellent isolation to variations in supply voltage when R_5 and R_6 are equal.

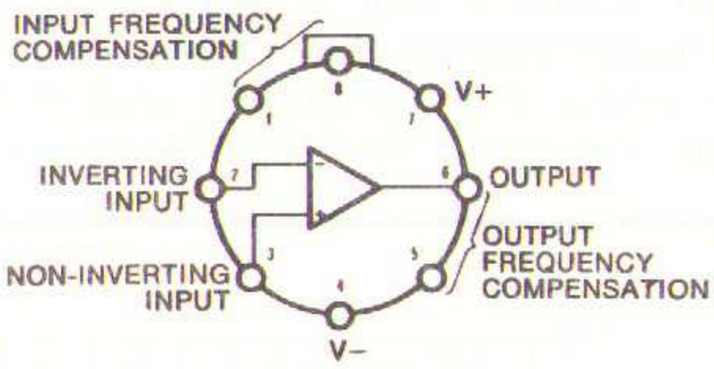
The actual circuit employed is shown in Fig. 2.32. A modified Darlington connection is used in the second stage to prevent loading of the input stage. This makes the second stage gain proportional to the predictable transconductance characteristic of the transistors, rather than the current gain.

A unique scheme is used to make the Darlington-connected second stage insensitive to high temperature leakages and stabilize it over the operating temperature range. This is shown in Fig. 2.31. The conventional way of accomplishing the task would be to connect a resistor across the emitter-base junction of TR_5. However, the required value of resistance would be large; and since the emitter-base voltage has a negative, and the resistor a positive temperature coefficient, the bleed current would become small at high temperatures where it is needed most and large at low temperatures where it is undesirable. However, with the scheme in Fig. 2.31, resistance values more than an order of magnitude lower can be used, and the bleed current has a strong positive temperature coefficient, as desired.

Schematic Diagram



To-5 Connection Diagram
(top view)



Note: Pin 4 connected to case.

Fig. 2.32 - Complete Circuit of the 709 Amplifier

As is clear from the figure, it uses the same principle as the input stage current source.

The remaining details of the second stage are that an emitter-follower, TR_7, is used to keep the input stage collector currents out of the collector of TR_5. Additionally, a second emitter-follower, TR_8, is used to prevent loading of the second stage by the output stage.

2.5.4. Output Stage

Level shifting to the output stage, Fig. 2.32, is accomplished using a lateral PNP transistor, TR_9, similar to that described in Section 2.1.2. It is made using what is usually an NPN base diffusion for an emitter. This is surrounded by a second base diffusion which serves as a collector. The normal NPN collector region is then the PNP base. This structure suffers from a rather wide base, displaying a low current gain (approximately 2). However, it has the distinct advantage that it can be made with the standard NPN process with no additional steps or control. The circuit is designed to operate satisfactorily with current gains lower than 0.2, so the device presents no problem in that the PNP will work well enough as long as the junctions are good.

A complementary, class-B output stage is used. The circuit has a built-in dead zone to prevent latch-up or runaway under overload conditions; each output transistor is positively turned off before the other is allowed to conduct. However, a large amount of internal feedback, through R_{15}, is used. This not only gives a low output resistance but also makes the crossover distortion almost indiscernible — even on the open-loop transfer function. An additional advantage of this scheme is that the output stage quiescent current is held to a minimum which helps the design objective of low power consumption.

A vertical PNP transistor is used in the output stage. This device uses the NPN base diffusion for an emitter and the P-type substrate of the integrated circuit for the collector (in the lateral PNP, this PNP action is suppressed by placing the N+ subcollector diffusion of the NPN underneath it). This PNP has a higher current gain than the lateral PNP but it also presents no problem as far as device yields are concerned since it need only function as a diode to meet circuit requirements.

Although it is not clear from the circuit, the output stage is actually short-circuit-proof. This characteristic is derived from the fact that the output transistors (TR_{14}, TR_{13} and TR_{12}) have small geometries (the whole integrated circuit is about the same size as output transistors that would normally be used). The current gain of these devices is injection-efficiency limited at high current levels. The injection-efficiency-limited current gain is relatively constant for a given process and geometry and falls off at high temperatures so this turns out to be a satisfactory method of short-duration current limiting.

Other details of the output stage are that R_{12} is used to make the circuit insensitive to leakages in TR_9 and TR_{12}. R_{13} reduces the internal loop gain of the output stage to stabilize the internal feedback. The gain of the output stage is essentially determined by the ratio of R_{15} to R_7, independent of the characteristics of the active devices.

2.6 SUMMARY OF 709 PERFORMANCE

2.6.1 Main characteristics of the 709 Integrated Amplifier

The typical performance of the 709 amplifier has been summarised in Table 3. Performance details, such as operating limits, parameters and maximum and minimum ratings can be obtained from the relevant data sheets, available upon request.

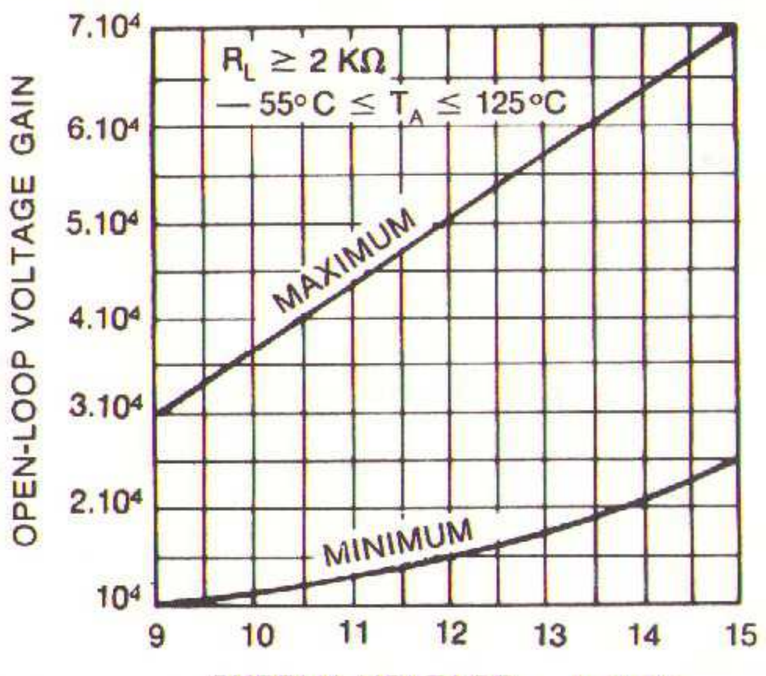


Fig. 2.33 - Voltage Gain as a Function of Supply Voltage

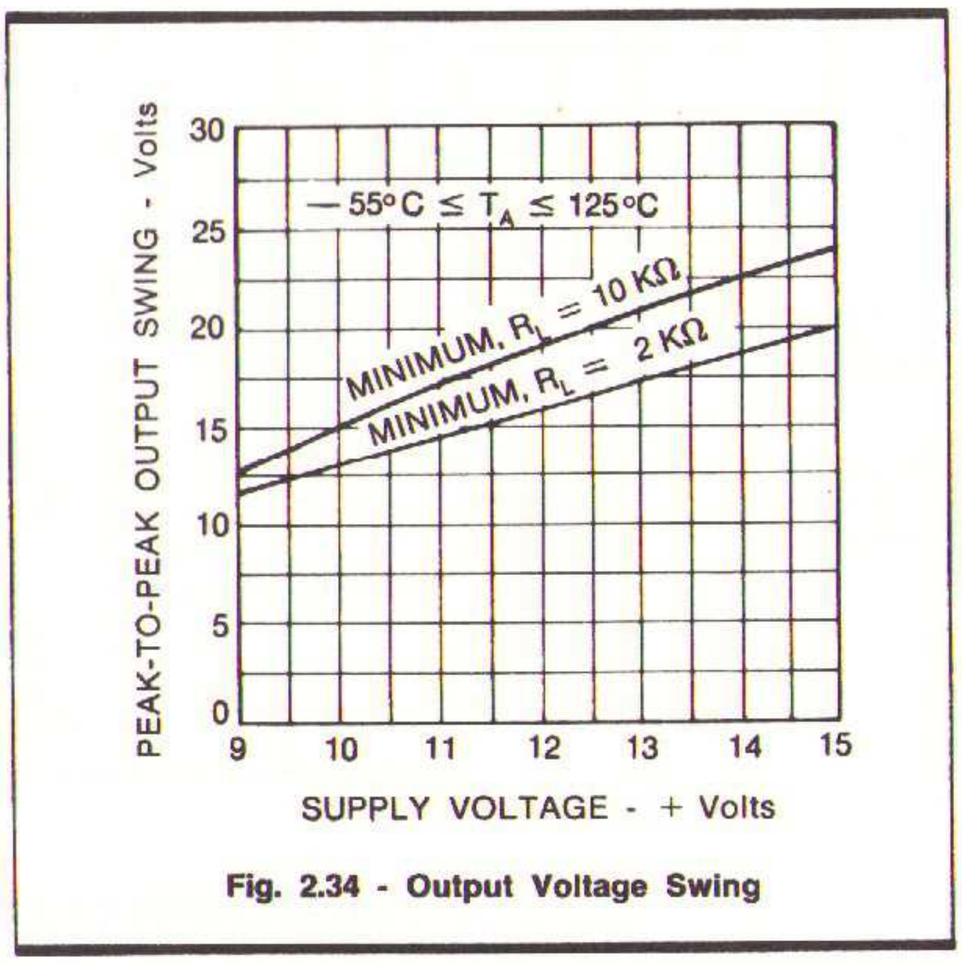


Fig. 2.34 - Output Voltage Swing

The amplifier can operate with a large variety of supply voltages, provided that both negative and positive voltages are kept equal to each other.

The open-loop voltage gain increases with supply voltage V_S, as shown in Fig. 2.33, this represents the maximum and minimum gain as a function of V_S.

Fig. 2.34 shows the minimum values of the maximum output swing which can be obtained with two values of load resistance. Fig. 2.35 and 2.36 show the allowable input common-mode voltage range and the increase of input current with the supply voltage respectively.

Since the transistor current gain increases with temperature, higher input resistance values and lower bias and offset currents are obtainable at high temperatures (see Fig. 2.37, 2.38 and 2.39 respectively).

The amplifier transfer characteristic (Fig. 2.40) shows the linearity and the output voltage swing of the 709. The « broken » curves represent the high

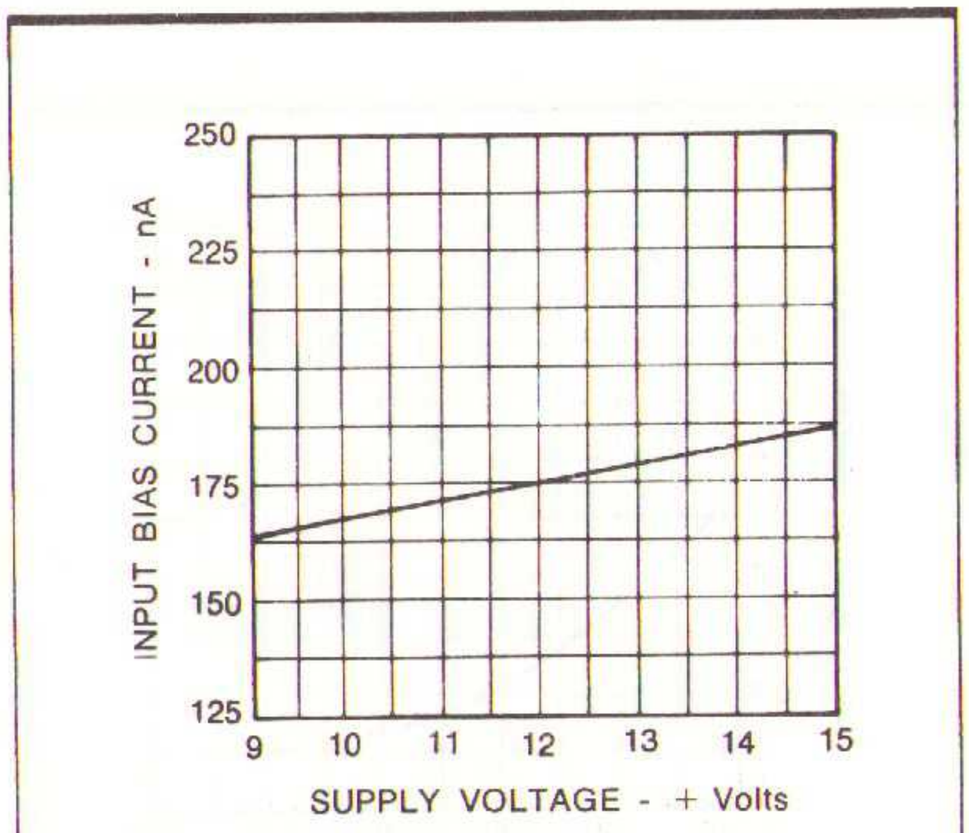


Fig. 2.36 - Input Bias Current as a Function of Supply Voltage

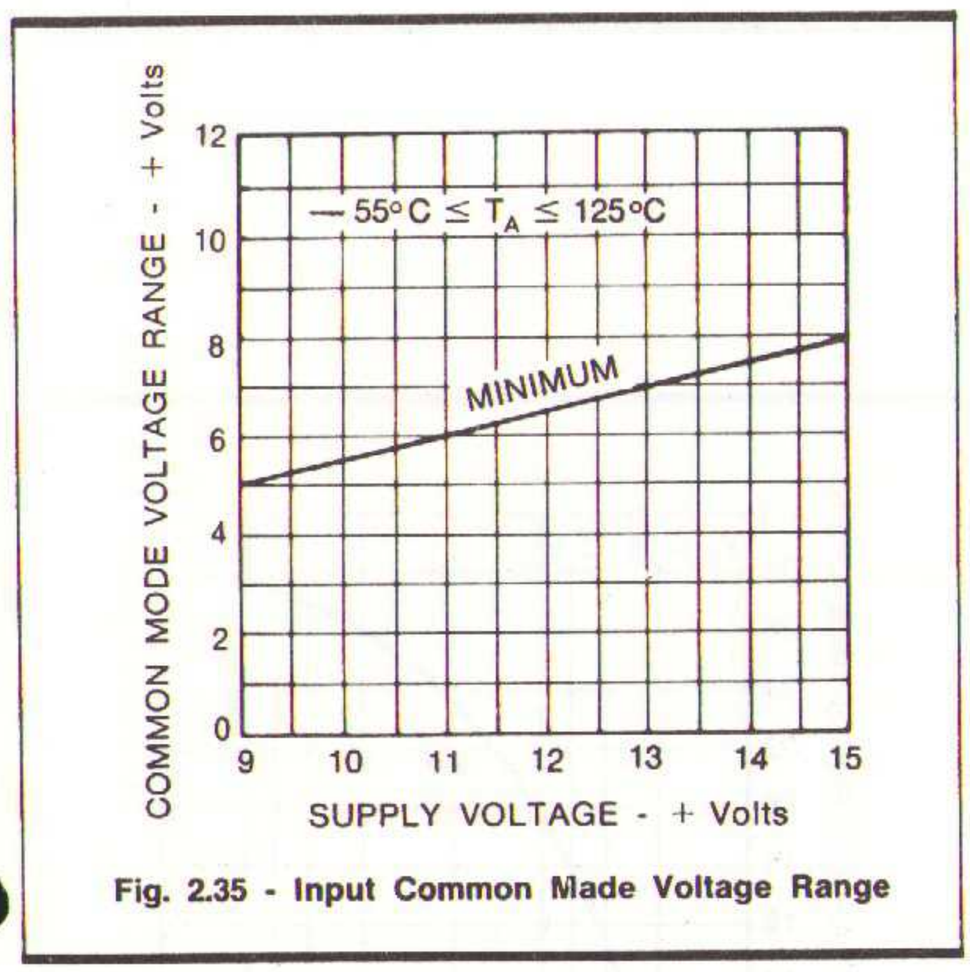


Fig. 2.35 - Input Common Made Voltage Range

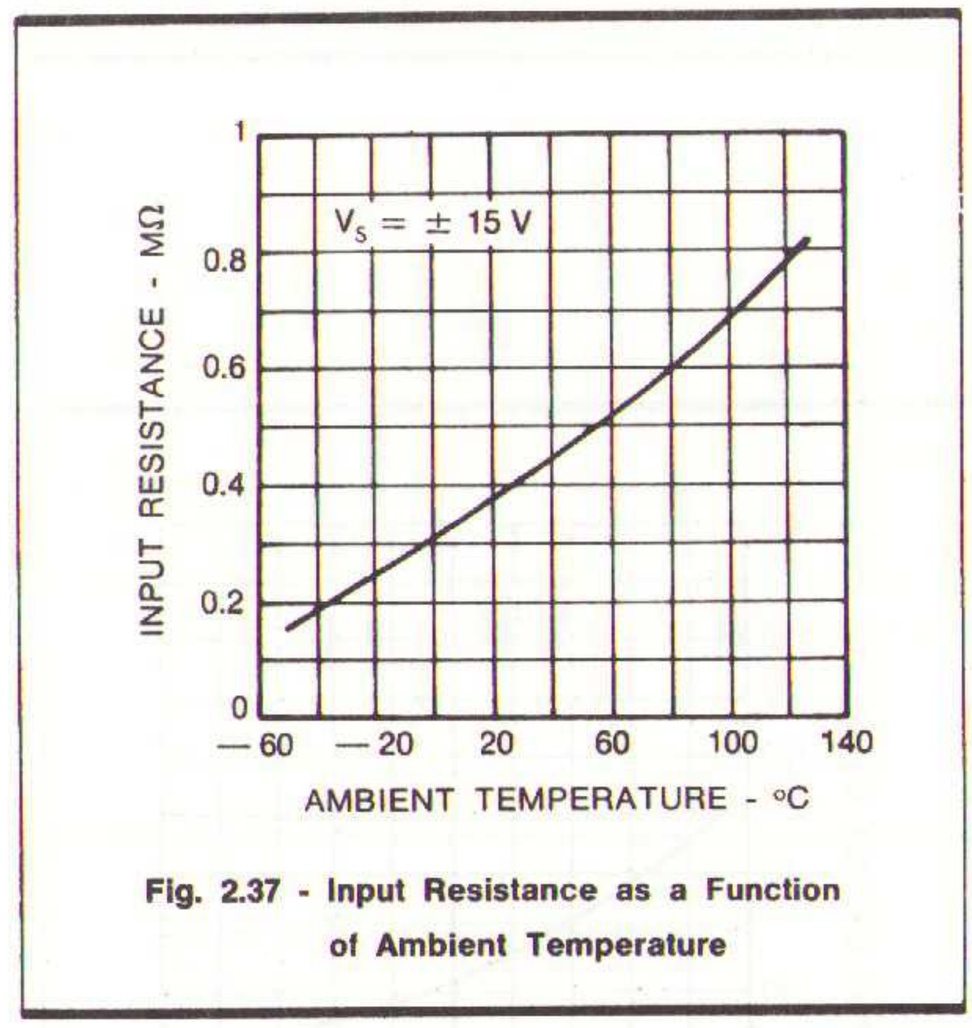


Fig. 2.37 - Input Resistance as a Function of Ambient Temperature

and low temperature transfer characteristics from which it is possible to see how the voltage gain decreases when the temperature increases.

Finally, the maximum output voltage swing as a function of the load resistance is shown in Fig. 2.41. The frequency characteristics and the noise performances of the integrated amplifier are examined separately in Sections 5.3 and 6.3.

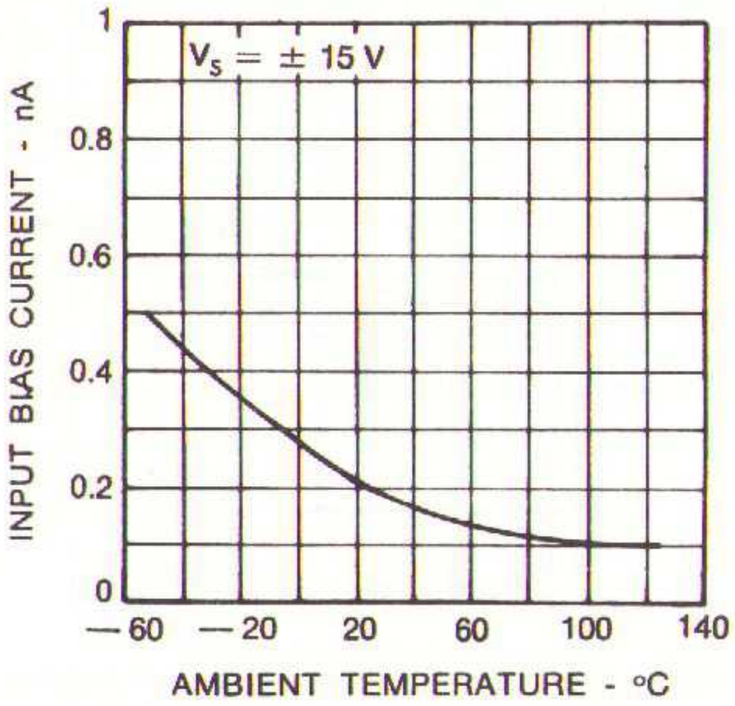


Fig. 2.38 - Input Bias Current as a Function of Ambient Temperature

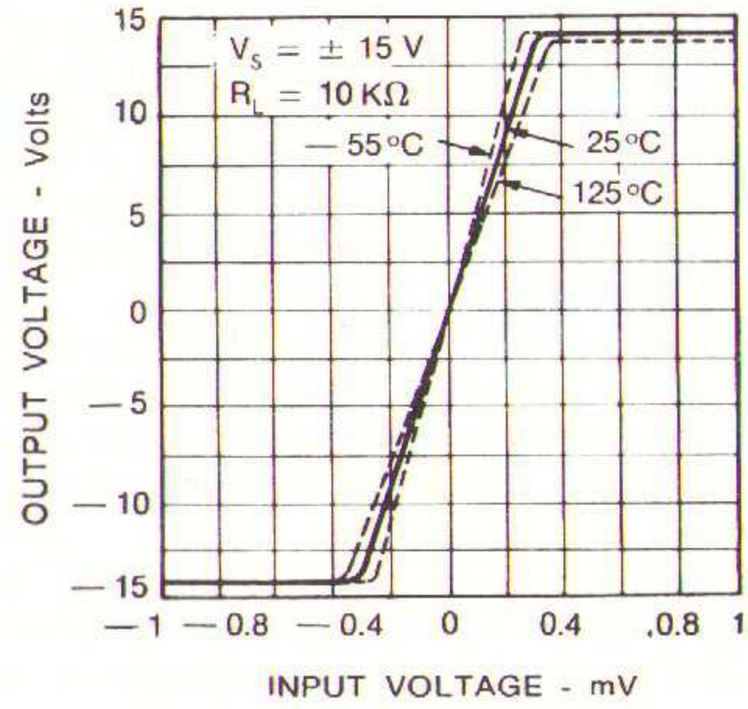


Fig. 2.40 - Voltage Transfer Characteristic

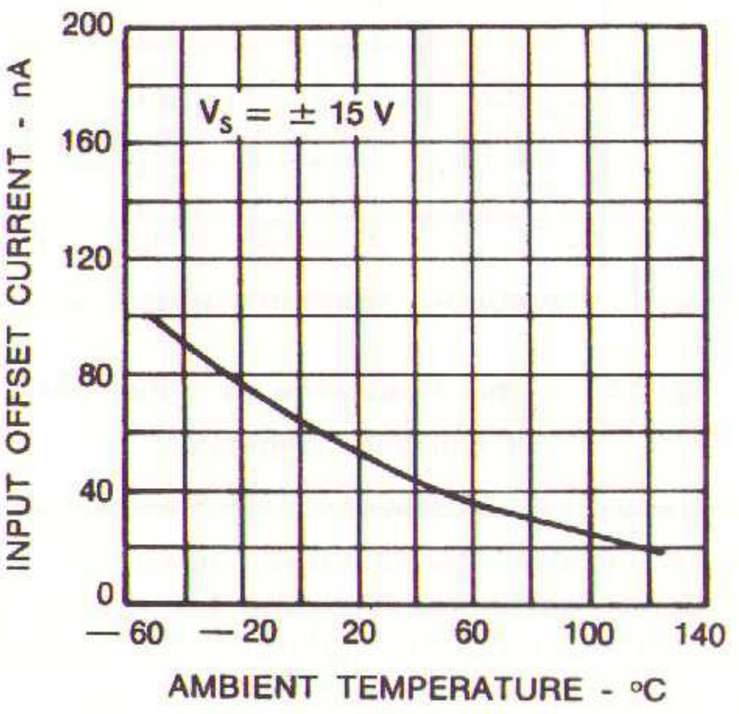


Fig. 2.39 - Input Offset Current as a Function of Ambient Temperature

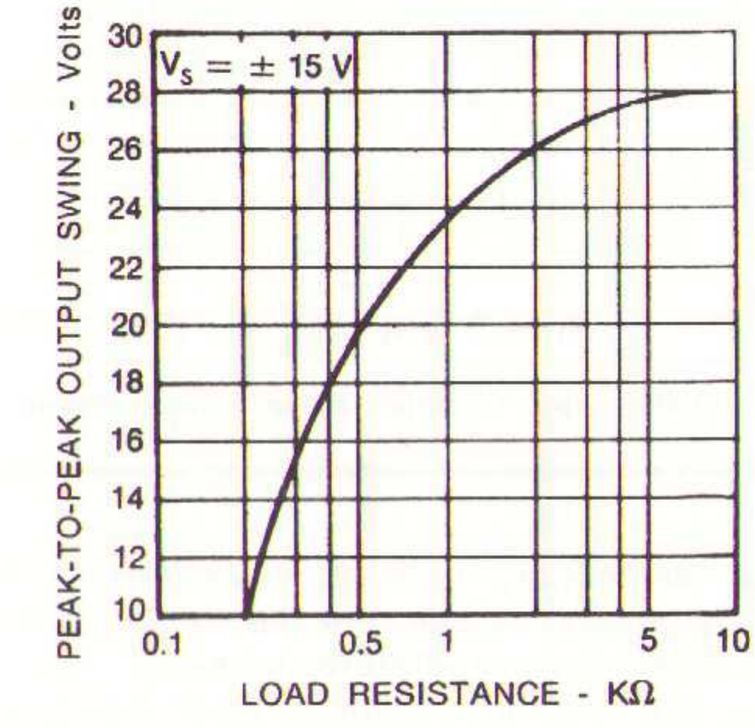


Fig. 2.41 - Output Voltage Swing as a Function of Load Resistance

Typical Conditions: $T_A = 25°C$, $\pm 9\,V \leq V_S \leq \pm 15\,V$ unless otherwise stated

Input Offset Voltage	1 mV
Input Offset Current	50 nA
Input Bias Current	200 nA
Input Resistance	400 kΩ
Output Resistance	150 Ω
Power Consumption	80 mW

The following specifications apply for $-55°C \leq T_A \leq 125°C$:

Large-Signal Voltage Gain	45000
Common-mode Rejection Ratio	90 dB
Input Voltage Range	± 10 V
Supply Voltage Rejection Ratio	25 μV/V
Voltage Drift	3 μV/°C

Table 3 - Typical Performance of 709 Amplifier

2.6.2 General Circuit Precautions

Use of the 709 under certain operating conditions can result in abnormal performance or catastrophic failure of the device. Since the source of the problem is not always immediately evident, the most common difficulties are dealt with in the following paragraphs. The protection schemes described may not be necessary in a well-designed system using the μA709, but can be used to good advantage in breadboard and bench work, where accidents are more likely to happen.

LATCH-UP

The common-mode voltage limits of the 709 are determined for negative inputs by saturation of the current source transistor, and for positive inputs by saturation of the input transistors. Exceeding the positive common-mode limit of the device may cause damage to the inputs through excessive current. Erratic operation can still result, however, even if the current is limited to a safe value. If the transistor on the inverting input saturates, for example, it no longer acts as an inverting amplifier but makes a direct connection between the input and the base of the second stage transistor — thus becoming a non-inverting input. This results in positive feedback, and latch-up will occur if it is possible for the output voltage to hold the input stage in saturation through the feedback network.

This tends to be a particular problem with the voltage-follower circuit of Fig. 2.42. It is easy for a transient to trigger latch-up since the output is connected directly to the inverting input. One possible solution is to put a 33 kΩ resistor between the output and input to limit the feedback current, but this increases the offset voltage. A better method is shown in Fig. 2.43. The output voltage is prevented from rising higher than the common-mode limit (voltage at base of TR_4 - Fig. 2.32, Section 2.5.3) by the diode clamp, D_1. This keeps the input transistor from going into saturation and hence latch-up can-

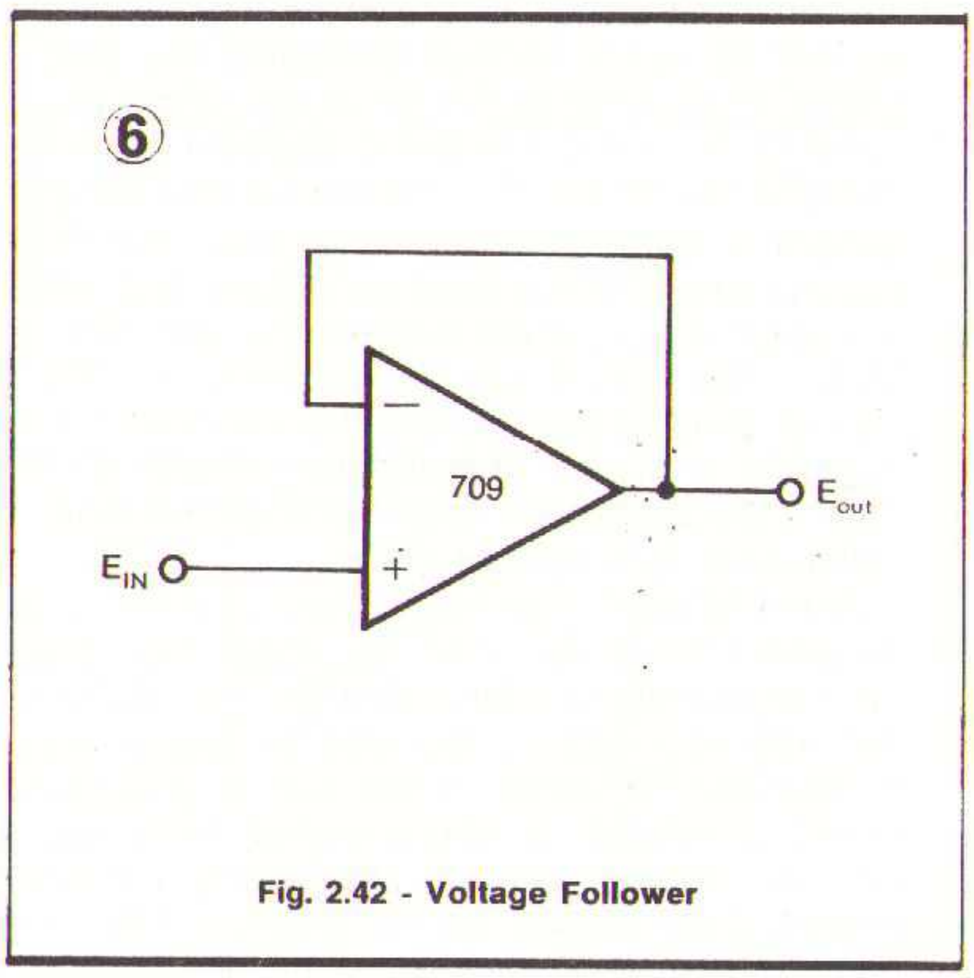


Fig. 2.42 - Voltage Follower

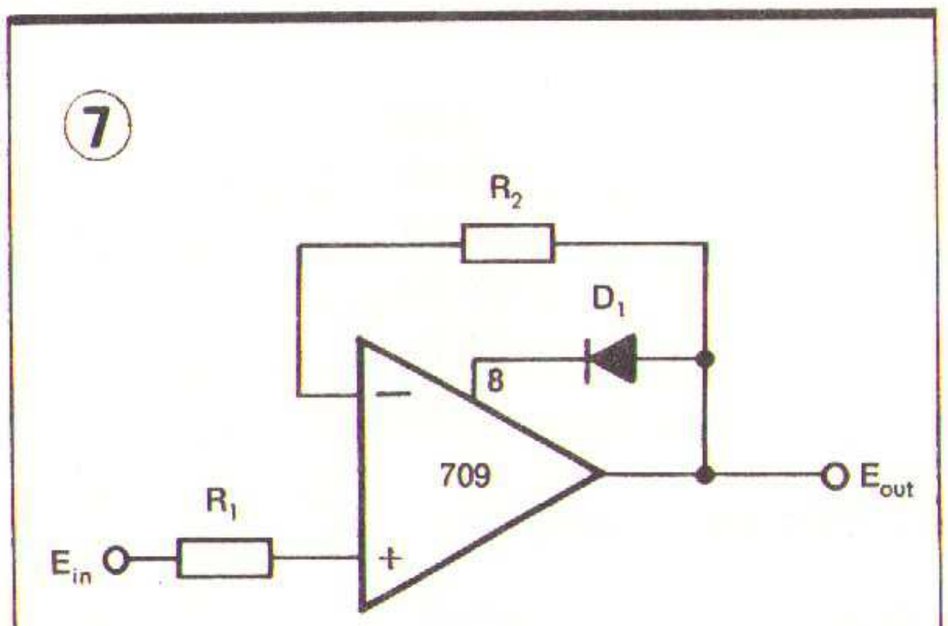


Fig. 2.43 - Protection Against Latch-Up

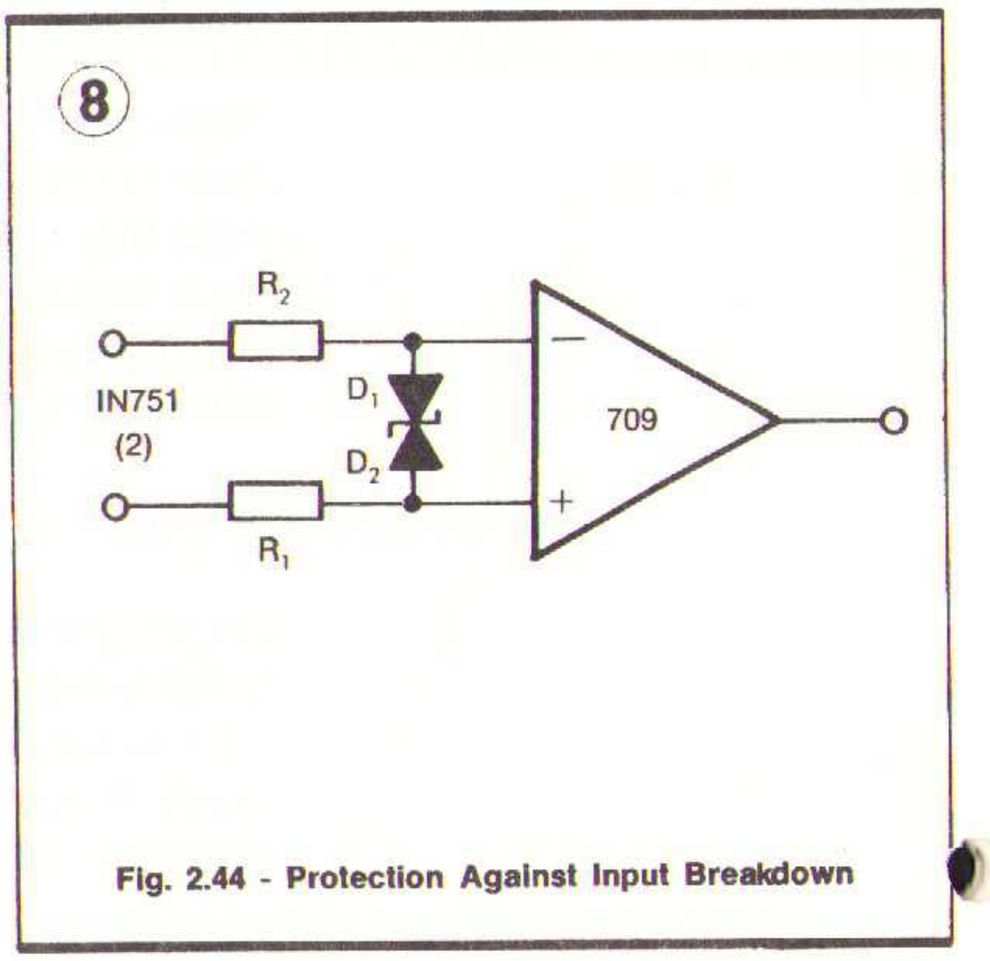


Fig. 2.44 - Protection Against Input Breakdown

not occur. Even though external resistors are not required to prevent latch-up with this circuit, it is wise to include some resistance at each input for protection against differential transients, as discussed subsequently. Up to 10 kΩ can be used without increasing the offset voltage above the guaranteed maximum.

DIFFERENTIAL INPUT VOLTAGE

Although the input common-mode voltage range of the 709 is a minimum of ± 8 V, the maximum voltage permitted between the inputs is limited to ± 5 V. If one of the inputs is grounded, for example, the other can only be driven as high as + 5 V or as low as — 5 V without exceeding the limit. It is important to observe this maximum rating since exceeding it could cause gross degradation in the input offset current, and input bias current, by drawing excessive current in breaking down the emitter-base junctions of the input transistors. The junctions will short if the current becomes greater than about 50 mA. The circuit can be protected by placing a pair of Zener diodes across the inputs as shown in Fig. 2.44, or a pair of fast silicon diodes as in Fig. 2.45, if the application does not require the full ±5 V differential input voltage range.

Some failures have been traced to the use of ungrounded soldering irons to install the amplifier. Line transients can feed through the insulation of the iron and destroy the unit by arcing over the emitter-base junctions. If the iron is grounded, the circuit grounded or disconnected from any line-operated equipment, and the supply voltages removed, there should be no problem. This type of damage can also be caused by ungrounded test equipment and temperature-chamber transients.

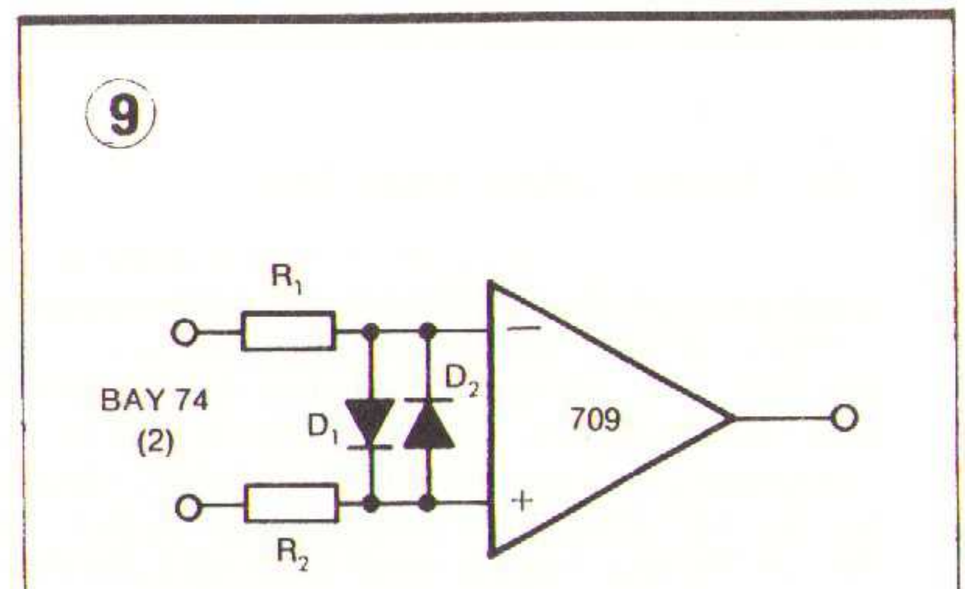


Fig. 2.45 - Protection Against Input Breakdown

SUPPLY VOLTAGE POLARITY

Another point that is sometimes overlooked is the polarity of the power supply voltages. It is quite important that the negative supply terminal always be the most negative point in a monolithic integrated circuit. If the supply voltages are reversed, the isolation diode that normally separates the different elements in the circuit becomes forward-biased. This effectively puts a short between the power supplies, resulting in a large current (greater than 750 mA) that melts the aluminium metallised interconnections. If the possibility exists that the supplies could be reversed, either by accident or by a turn-on transient in the power supply step-up, the amplifier can be protected with a diode as shown in Fig. 2.46.

OUTPUT SHORT-CIRCUIT

As explained in Section 2.5.4, the output stage of the 709 can withstand a short-circuit for a short period of time. The current gain of the output transistors is injection-efficiency limited at high current levels and falls off at high temperatures. This limits the short-circuit output current to about 75 mA for any condition of input drive. The length of time that the device can survive a direct short is a function of the internal power dissipation and temperature, and is at least 5 seconds at 25°C.

Protection against short-circuits to ground of any duration can be made by inserting a small resistor in series with the output to limit the maximum power dissipation. At the expense of a 10% reduction in maximum output voltage swing (into a 2 kΩ load), the 200 Ω resistor shown in Fig. 2.47 will completely short-circuit protect the amplifier for ambient temperatures to 75°C. The resistor does not affect the normal operation of the circuit since it is inside the feedback loop.

If the 709 is used to drive logic integrated circuits it is important to limit the maximum output swing of the amplifier, otherwise damage could occur at the input of the logic integrated circuits.

Fig. 2.48 shows a method which effectively overcomes these problems.The diode D_1 prevents negative excursions of the amplifier which exceed approximately — 0.7 V.

The diode D_2 connected to the positive logic supply will prevent the output voltage from becoming greater than the logic supply. Finally, the resistor R_2 in series with the output limits the maximum power dissipation of the 709.

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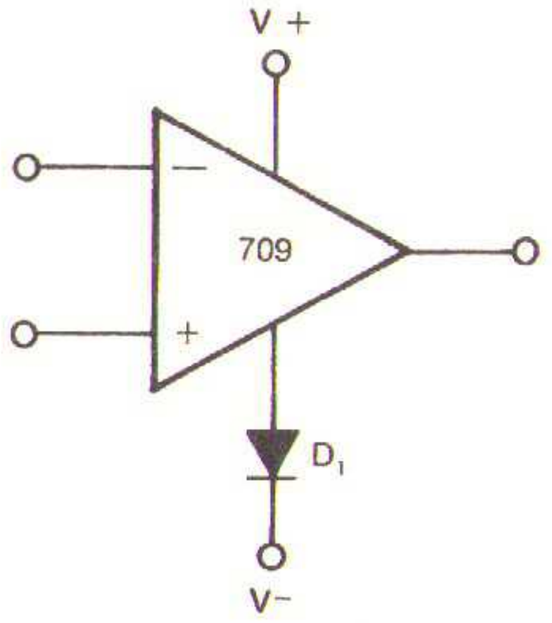

Fig. 2.46 - Protection Against Power Supply Reversal

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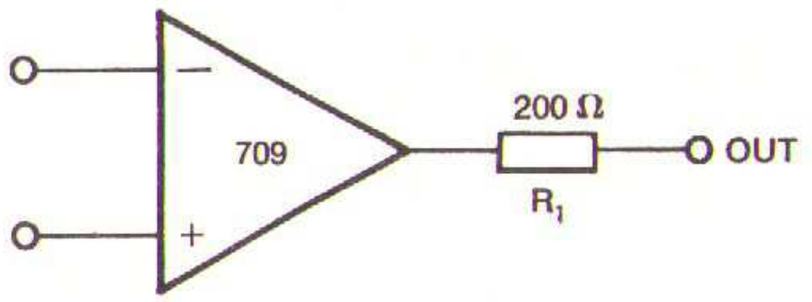
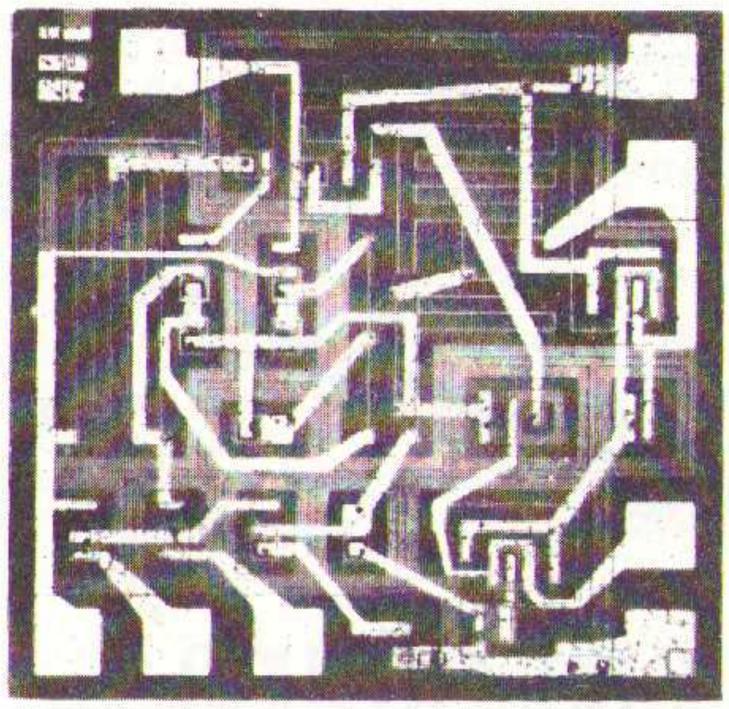


Fig. 2.47 - Protection Against Output Short-Circuit



- Photomicrograph of the SGS μA709 High Performance Operational Amplifier

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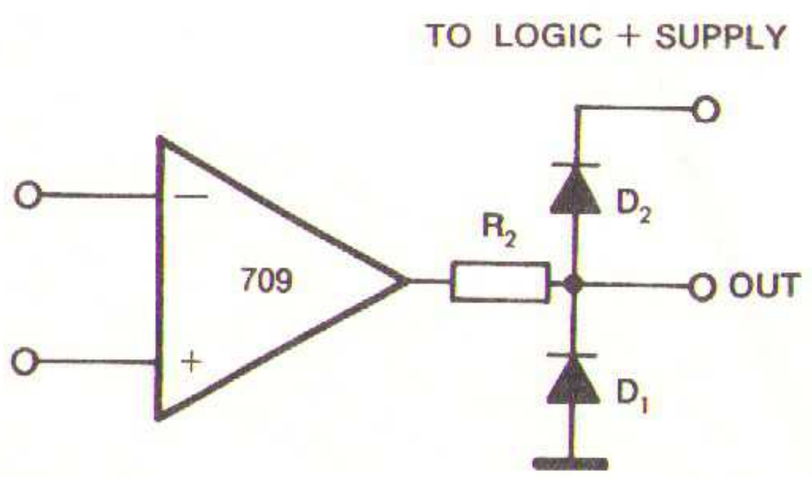

Fig. 2.48 - Logic Compatibility

A A N T E K E N I N G E N

N O T E S

MEASUREMENT OF INTEGRATED CIRCUIT BASIC PARAMETERS

4.1 INTRODUCTION.

This section describes fairly simple test circuits which may be used either to investigate in greater detail certain integrated circuit parameters, for example, the effects of variation in temperature or power supply voltage on offset current, open loop gain, ect., or merely to check that a suspected device is still functional and conforms to specification.

In order that better use may be made of the described circuits, it is strongly recommended that the other sections of this technical documentation are read first, in particular the section on frequency compensation.

4.2 TEST CIRCUITS.

General Functional Test.

The measure of large signal gain, linearity and output voltage swing can be found from the amplifier open-loop transfer function, which is a display of the input/output characteristics of the circuit over its full dynamic range.

The transfer function is obtained by applying the A.C. input and output signals of the device under test to the horizontal and vertical inputs of the oscilloscope, respectively.

The resultant oscilloscope trace is a plot of the amplifier output versus input: maximum output voltage swing, linearity and gain can be determined from the curve, shown in Fig. 4.1.

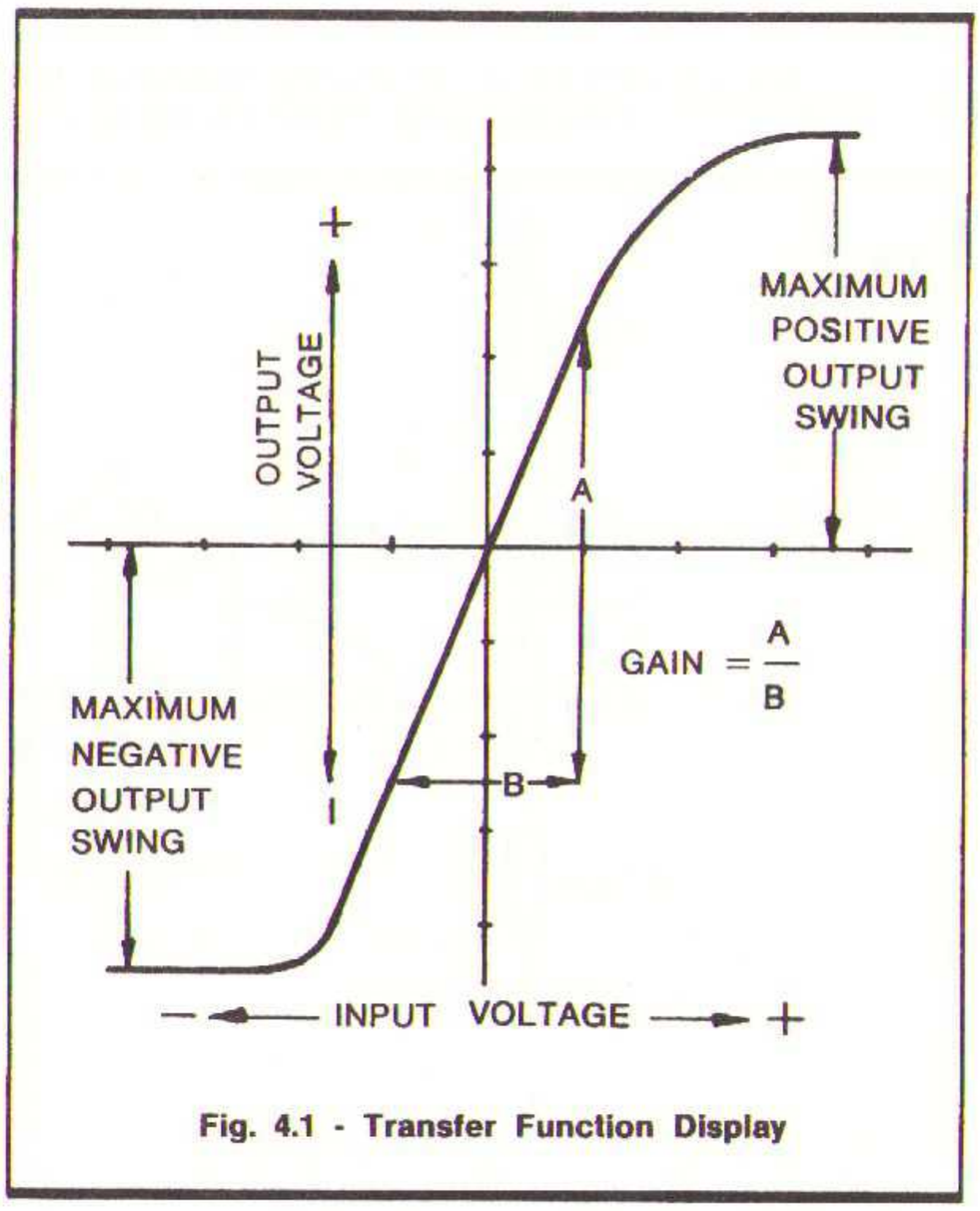

Fig. 4.1 - Transfer Function Display

The basic circuit for the 709 is shown in Fig. 4.2.

D.C. stabilisation of the operating point for the amplifier must be provided; this is because the D.C. gain is very high and an offset of a few millivolts is enough to hold the output in saturation over part or all of the input cycle.

The amplifier is effectively tested under open-loop conditions, since at frequencies above 1 kHz the reactance of C2 is negligible when compared to R4. Both C1 and C2 should be of low leakage type and capable of efficient operation at high frequencies. Solid tantalum or ceramic types are suitable.

The A.C. signal for the transfer function is applied to the input of the device under test through a precision attentuator (R1, R2).

The need for a high-gain horizontal deflection amplifier is eliminated by connecting the horizontal input of the oscilloscope to the high-level terminal of the divider.

Common-mode Rejection Ratio and Input Voltage Range.

The common-mode rejection ratio is defined as the ratio of the input voltage range to the maximum change in input offset voltage over this range, and the input voltage range as the range of voltage on the input terminals for which the device will operate within specifications. Fig. 4.3 shows the circuit suitable for measuring the above-mentioned parameter for the 709.

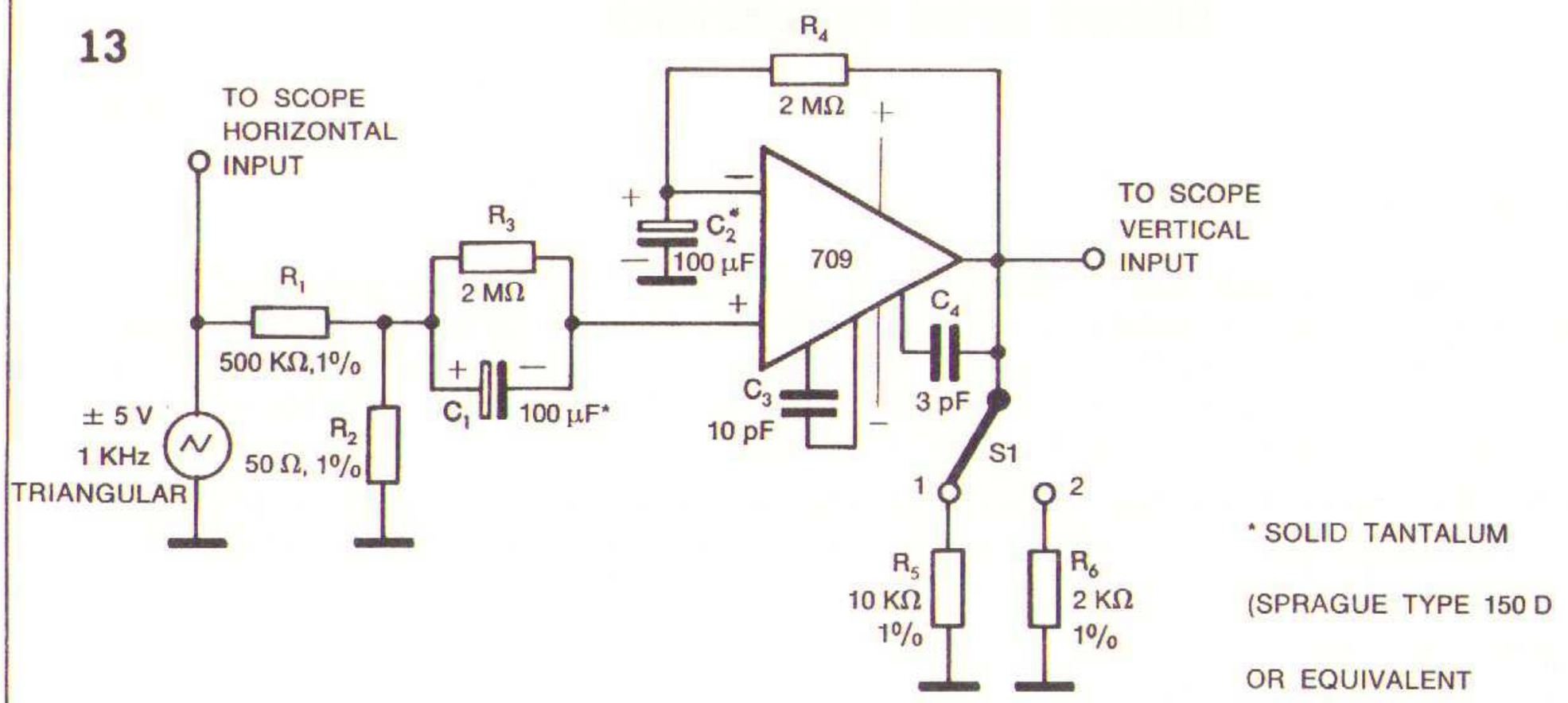

Fig. 4.2 - Circuit for Displaying Open-loop Voltage Transfer Function, Measures Output Voltage Swing, Open-loop Voltage Gain

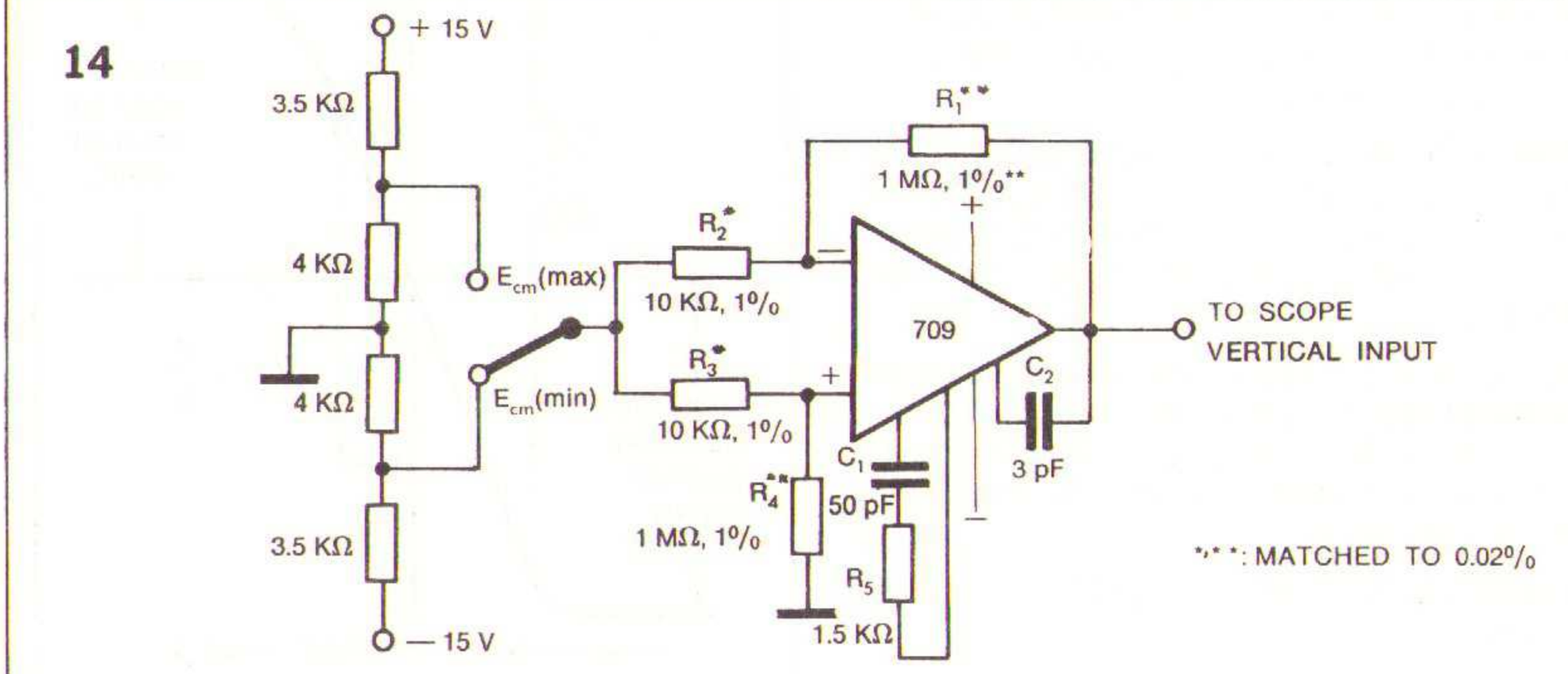

Fig. 4.3 - Circuit for Measuring Input Common Mode Rejection Ratio and Input Voltage Range

Resistors R2, R3 and R1, R4 set the amplifier voltage gain Af to 100 and provide the D.C. current path to the input. These resistances must be closely matched otherwise different tolerances will affect the test.

For the 709 the input signal change is symmetrical between +8 and -8 volt (which is the minimum guaranteed input voltage range) and the common-mode rejection ratio (CMRR) is given by:

$$CMRR = \frac{1600}{\Delta Vout}$$

It is usual to express this ratio in dB and therefore this formula would be given by:

$$CMRR = \frac{1600}{\Delta Vout}\,.$$

For a supply voltage lower than ± 15 volt proportionally less signal amplitude should be used.

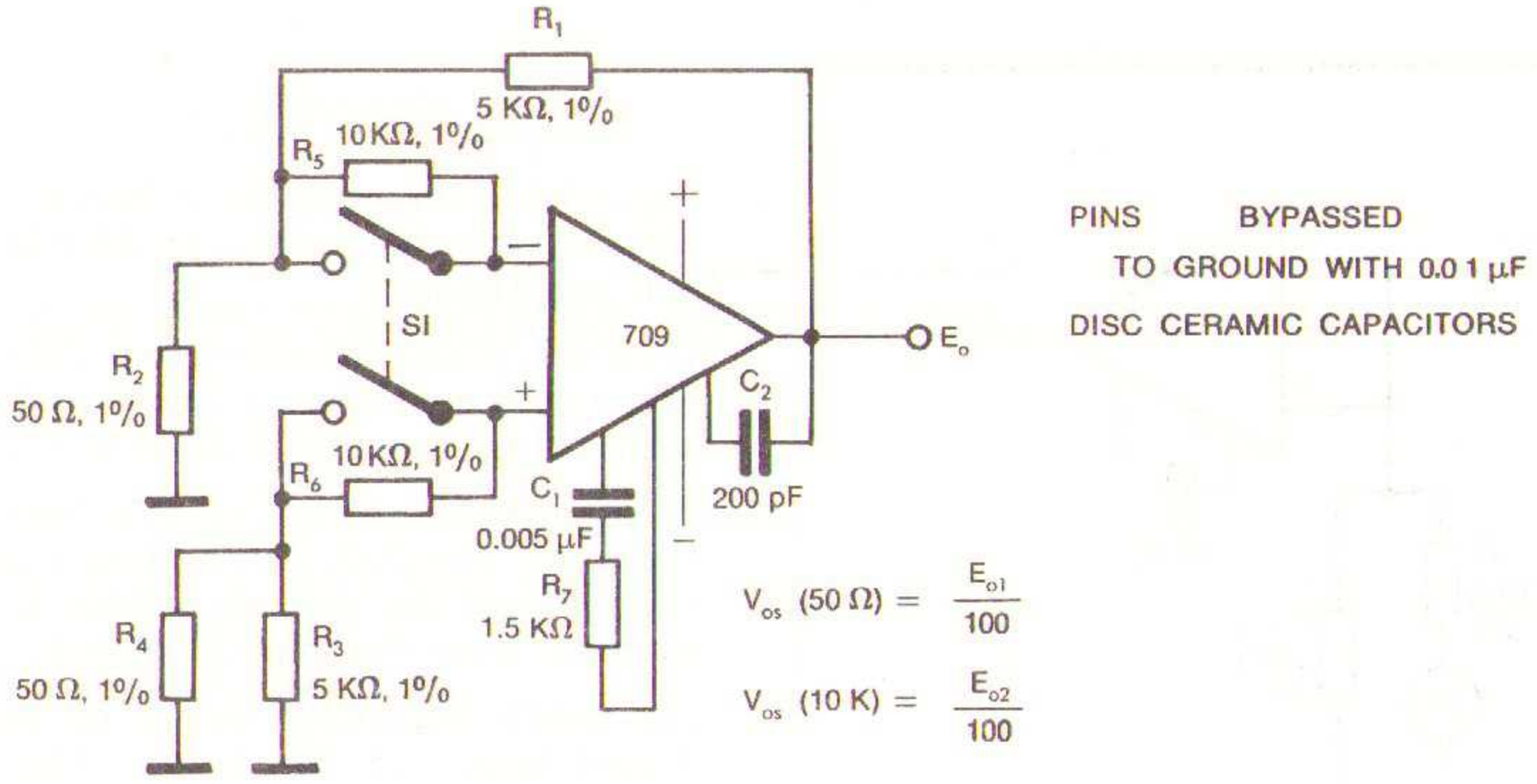

Fig. 4.4 - Circuit for Measuring Input Offset Voltage and Power Supply Sensitivity

Input Offset Voltage.

The input offset voltage is defined as the voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistors are connected in series with the input leads.

Fig. 4.4 shows the circuit to measure this parameter for the 709. For good sensitivity it is preferable to make R1 at least 100 times greater than R2, so that the oscilloscope or digital voltmeter used to read the output will be able to operate on a convenient range.

Resistor R2 should be kept at the lowest feasible value to prevent current offset from superimposing its effect on the voltage offset measurements, 50Ω is a suitable value.

The input offset voltage is obtained by $V_{offset} = V_{out} : 100$.

When S1 is open, the effective sourse resistance is increased bij 10kΩ for the 709.

Input Offset Current.

Input offset current is the difference between the currents into two input terminals at zero voltage. Fig. 4.5 shows the circuit to measure the input offset current for the 709.

The D.C. output voltage is given by: $V_{out} = I_{offset}R2 + V_{offset}$. Obviously the source resistance R2 = R1 is chosen so that the term $I_{offset}R2$ is greater than the voltage offset: in such a condition the above-mentioned relation becomes:

$$I_{offset} = V_{out} : R2.$$

The capacitors C1 and C2 should be of very low leakage type and capable of efficient operation at high frequencies.

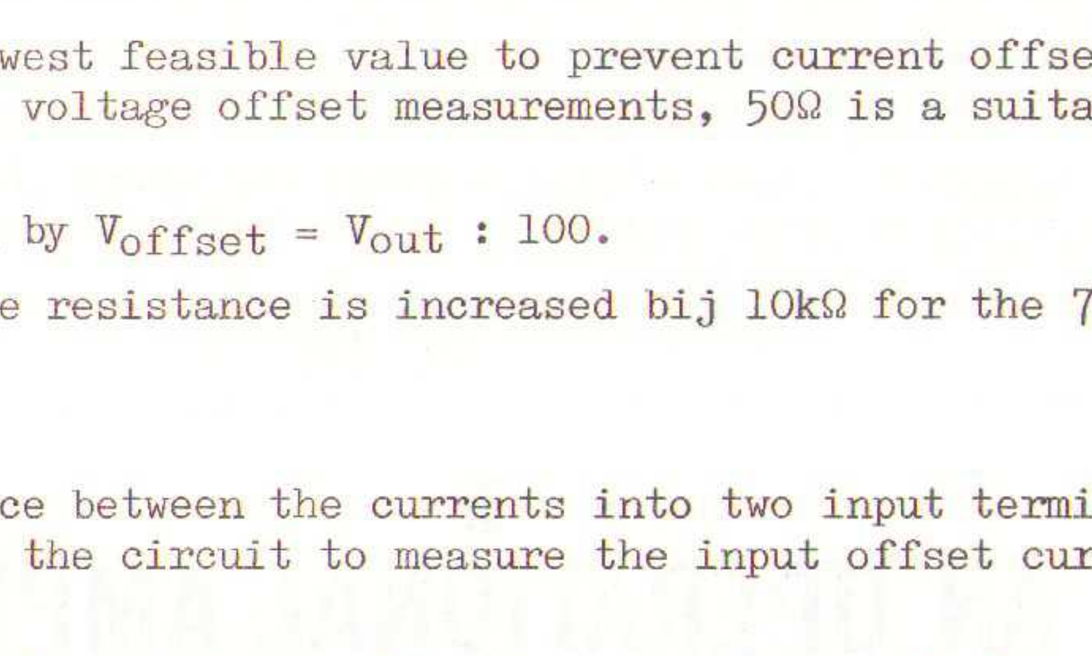

Fig. 4.5 - Circuit for Measuring Input Offset Current

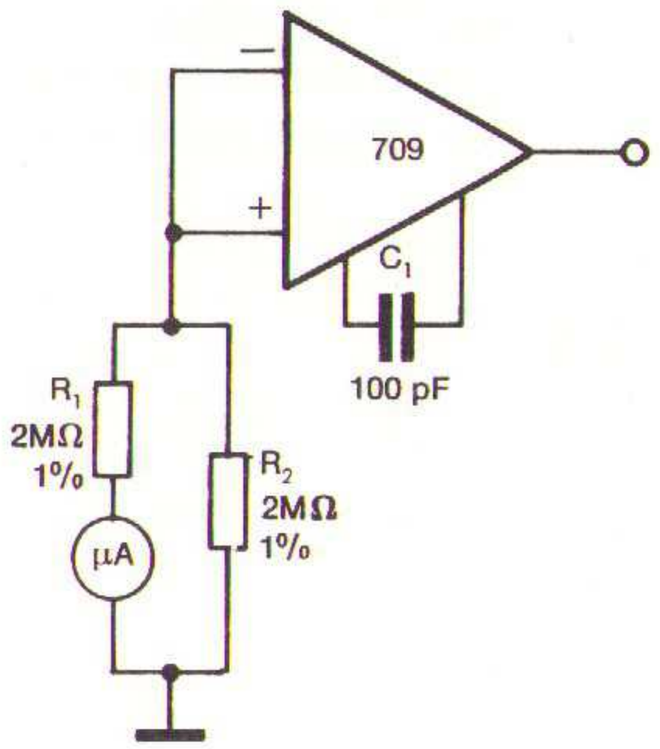

Fig. 4.6 - Circuit for Measuring Input Bias Current

Input Bias Current.

Input bias current is defined as the average between the two currents flowing into the input terminals.

This value may be obtained using a D.C. current meter connecting in series with one of the two paralleled resistors R1 and R2.

If R1 and R2 are equal and the internal resistance of the D.C. current meter is much lower than R1 and R2 the resistors divide the input current into two equal halves.

The meter indicated value is therefore the direct value of the bias current.

Bias current is defined for a certain value of supply voltage and at a fixed ambient temperature.

Supply Voltage Rejection Ratio.

Defined as the ratio of the change in input offset voltage to the change in supply voltage producing it.

The circuit Fig. 4.4. may be used to measure this parameter.

The positive or negative supply, or both, are varied by a known amount Vs ($\pm$ 10% of nominal value would be reasonable).

The change in input offset voltage expressed in microvolts is read and the value of the Supply Voltage Rejection Ratio (SVRR) is calculated from the relationship

$$SVRR = \frac{\Delta V_{offset}\ (\mu V)}{\Delta Vs\ (V)}.$$

AN OPERATIONAL AMPLIFIER TESTER

A simple and inexpensive tester for Motorola's line of operational amplifiers is described which will measure the open loop voltage gain, the equivalent input offset voltage, the maximum positive and negative output voltage swing, and a view of the transfer function which shows the linearity of the device.

Included is an elementary discussion of the parameters measured and their relationship to closed loop performance.

AN OPERATIONAL AMPLIFIER TESTER

INTRODUCTION

The primary purpose of this paper is to provide the customer with a simple and inexpensive tester for I/C operational amplifiers. It was designed to be easy to build and retain the accuracy necessary for the majority of testing.

This paper is prompted by customer inquiries for an operational amplifier tester that would check the devices and give the customer a degree of confidence that the units are functioning satisfactorily. Herein lies the reasoning for the choice of measuring the open loop voltage gain (A_{VOL}), the equivalent input offset voltage (V_{io}), the output voltage limits ($V_{o\ max}$, + and -), and the transfer function. Determining these parameters will normally cover the majority of constraints for an intended application.

The versatility of the tester is accentuated by the relative ease of adding test sockets for other devices.

THE TEST FIXTURE

As with most any tester, there must be provided a drive circuit, a power source, a device under test (D. U. T.) adapter, and a display unit. These are shown in the block diagram, Figure 1.

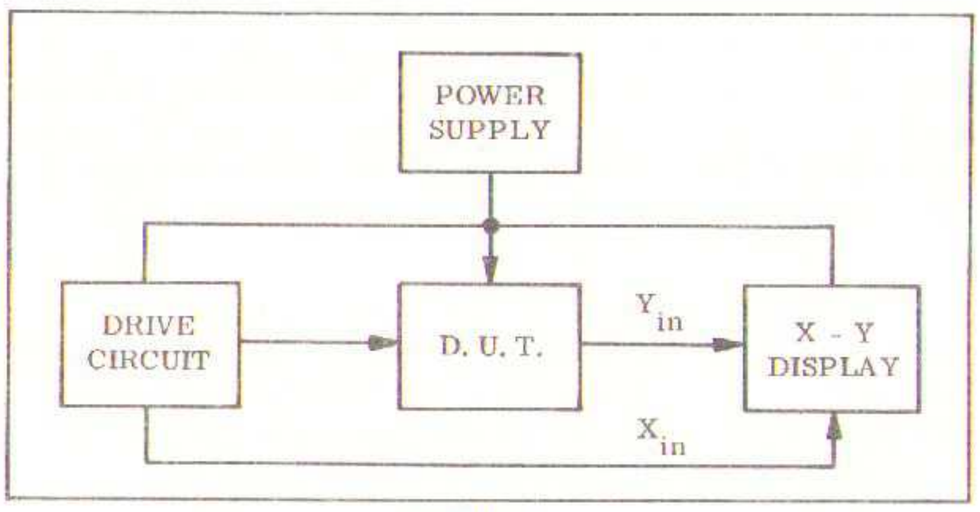

FIGURE 1

Since the incorporation of a display unit would duplicate the function of an X-Y oscilloscope which is usually available in most laboratories, this function was not included in the tester.

DISCUSSION OF THE TESTER

The power supply shown in the schematic of Figure 2 is a straight-forward shunt zener regulated power supply. The pilot lamp is bridged across the filtering capacitors as an on-off indicator and as a bleeder to remove the capacitor charge after power is turned off. The resistive divider in the transformer secondary serves as the input to the drive circuit.

The drive circuit is shown in Figure 3. The requisite of the drive circuit is that the vertical drive signal and the horizontal sweep signal are synchronized and identical in characteristics.

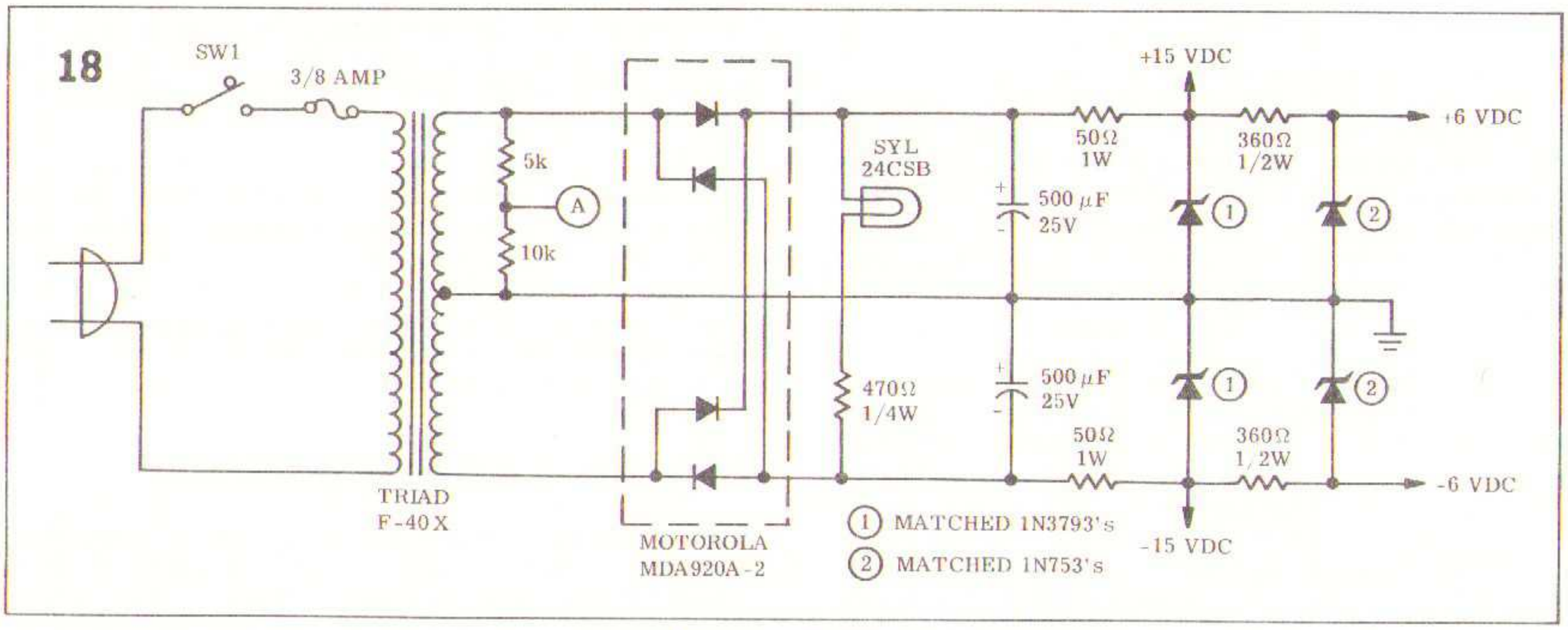

FIGURE 2 — POWER SUPPLY

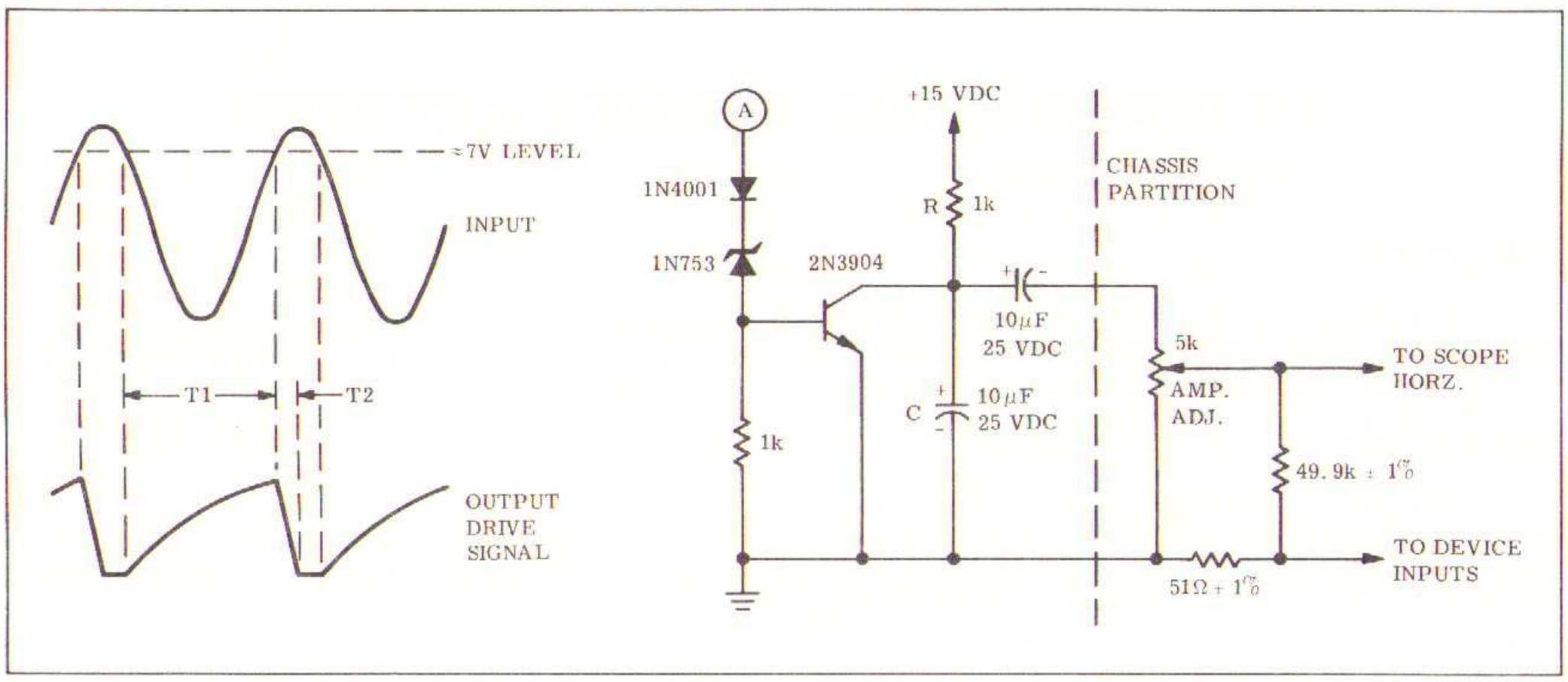

FIGURE 3 — DRIVE CIRCUIT

The most straightforward way of accomplishing this is to drive the DUT input and the horizontal sweep with the same signal. Realizing that the DUT, which in this case is op amps, will have a gain normally exceeding 1000, a 1000 to 1 precision resistive divider is placed at the input of the DUT. This brings into line the relative amplitudes of the X and Y inputs presented to the scope. For devices which exhibit much greater gains, say greater than 100,000, another divider could be added. At this level, it is recommended that the divider be placed at the individual test socket to lessen the possibility of interference on the line.

It is desirable, although not necessary, that the retrace not appear on or be blanked from the visual presentation. This is accomplished by the drive circuit by "intensity modulation," i.e. the relative intensity of the scope trace is determined by the sweep rate, given a fixed set of other trace variables.

The operation of the drive circuit, Figure 3, is simple. While the transistor is off the RC combination indicated is permitted to freely charge toward the +15 Vdc power supply. The time constant was chosen such that an ample amplitude resulted while deleting the more exponential portion of the charge curve. It should be evident that the time constant must be sufficiently longer than the period of the reset rate which in this circuit is 60 Hz.

A portion of the power transformer secondary voltage is used as the drive circuit input. As the input sine wave exceeds a predetermined threshold voltage (approximately $2V_{BE} + V_Z$) the transistor is turned on hard, discharging the timing capacitor. This results in the waveform shown in the inset of Figure 3. This waveform is then AC coupled to the DUT's, via the amplitude adjust and divider, so that their inputs are apparently driven from minus to plus voltages. As seen in Figure 3 inset, the relative intensity of the trace and retrace are determined by the ratio of T_1 to T_2. Therefore, with the scope intensity properly adjusted, the retrace does "disappear."

The difference between the horizontal and vertical drive voltages is a precise 1000 to 1 ratio. This permits the horizontal sweep voltage to be of sufficient magnitude, while retaining the ability to read V_{io} accurately.

The wiring of all DUT sockets is shown in Figure 4. Proper hook-up and frequency roll-off are required. Power supply terminals should be bypassed at each socket. A single 2 kilohm resistor is used as a common load for all devices. The exact test load can be tailored individually, if desired.

The "30-31" switch is required in order to use the same socket for MC1530/MC1430 and MC1531/MC1431 Plastic Dual In-Line Package, since their inputs are on different pins. A switch is also provided for the hi-lo gain option of the MC1433/MC1533.

Additional DUT sockets for other devices can be incorporated as the demand warrants. The maximum drive signal available is 8 volts peak to peak open circuit from the 5 kilohm amplitude adjust pot. This is believed to be wholly sufficient for most devices available.

In order to add other DUT sockets, it is only necessary to install the desired configuration, condition the signal drive amplitude as needed, and route the device output to the scope vertical input. Keep in mind that the amplitude of the device signal input must be sufficient to overcome any input offset voltage as well as driving the device into deep saturation.

DISCUSSION OF MEASURED PARAMETERS

Open loop voltage gain (A_{VOL}) is defined as the ratio of a change in output voltage to a change in input voltage at the input terminals. Ideally, for an operational amplifier, this parameter should be infinitely high since the primary function is to amplify and, in general, the higher the gain the better the gain accuracy. The significance of open loop gain is many times misapplied in amplifier operation where in reality open loop gain determines closed loop accuracy limits rather than the ultimate accuracy.

Referring to Figure 5 which contains a somewhat ideal operational amplifier, the closed loop gain of the circuit is:

$$e_o = - \frac{A_{VOL} \quad \frac{R_2}{R1 + R2}}{1 + A_{VOL} \quad \frac{R_1}{R1 + R2}} \qquad (1)$$

If the amplifier of Figure 5 exhibited infinite open loop gain, equation 1 reduces to

$$e_o = - \frac{R2}{R1} \qquad (2)$$

the ratio of two passive elements, which is the ideal closed loop gain of an operational amplifier connected in this mode of operation. The error in the closed loop gain (ϵ_{CL}) of an amplifier may be represented as:

$$\% \epsilon_{CL} = \frac{\frac{e_o}{e_{s\ IDEAL}} - \frac{e_o}{e_{s\ ACTUAL}}}{\frac{e_o}{e_{s\ IDEAL}}} \times 100 \qquad (3)$$

which after insertion of equations 1 and 2 reduces to

$$\% \epsilon_{CL} = \frac{100}{1 + A_{VOL} \quad \frac{R_1}{R1 + R2}} \qquad (4)$$

MC1530/31
MC1430/31

MC1533
MC1433

MC1709
MC1709C

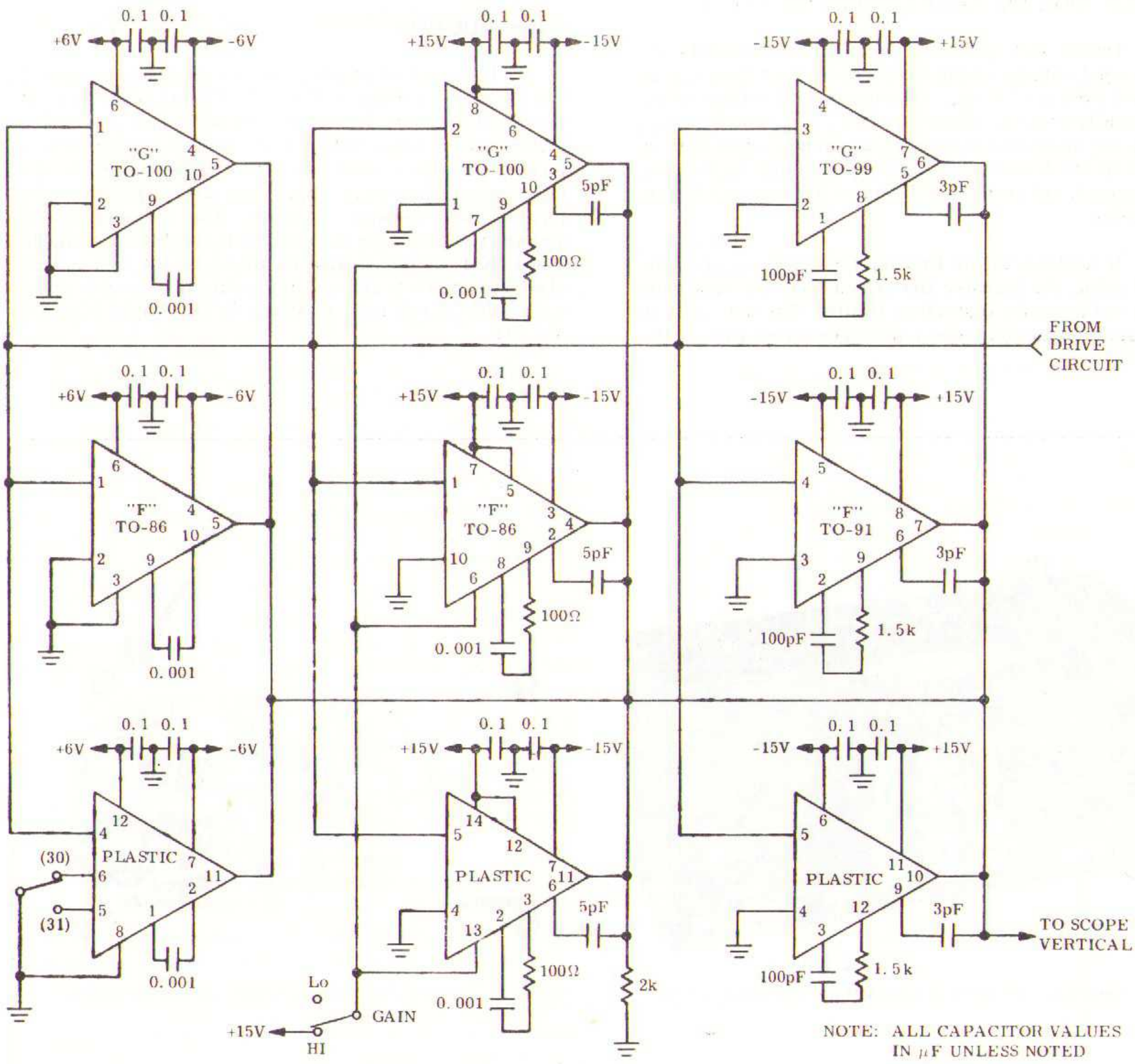

FIGURE 4 — DEVICE UNDER TEST SOCKETS

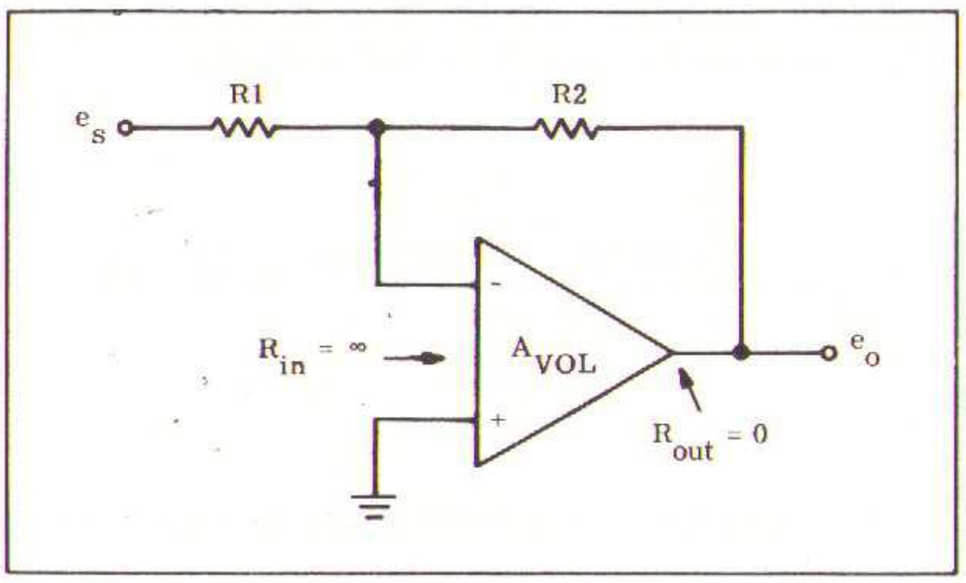

FIGURE 5 — IDEALIZED OPERATIONAL AMPLIFIER

The closed loop gain error is a direct function of the loop gain $(A_{VOL} \frac{R_1}{R_1 + R_2})$ rather than solely open loop gain. Open loop gain is the limiting factor in closed loop gain error; loop gain establishes the accuracy.

Output voltage swing ($V_{o\ max}$) is defined as the peak output voltage swing referred to zero that can be obtained without clipping. A symmetrical voltage swing is generally implied. However, if $V_o^+ max$ and $V_o^- max$ differ, the maximum symmetrical voltage swing will be limited by the lesser absolute value. Output impedance, load current, and frequency directly effect this particular parameter.

In addition to the limiting factor ($V_{o\ max}$) to the output swing, the transfer linearity affects the maximum output swing within distortion limits. The deviation of the transfer function from a perfect straight line, within the saturation limits, is indicative of the degree of distortion that can be expected in the output signal as well as the peak voltage at which this distortion occurs.

Input offset voltage (V_{io}) is defined as that voltage that must be applied at the input terminals to obtain zero output voltage. This parameter is also indicative of matching tolerances in the differential amplifier stages. It is primarily determined by the V_{BE} difference in the input stage and unbalance in the second stage attenuated by the gain of the first stage. In general this parameter will be the major source of offset voltage error in low source impedance circuits. Those devices with minimal V_{io} are better matched and would generally track well with temperature variations and, therefore, would exhibit minimal output drift with temperature variations. A factor not always considered when determining the contribution of V_{io} in closed loop operation is that this error is not simply increased by the ratio of feedback resistance to input summing resistance, but by unity plus this ratio. At higher closed loop gain levels, the difference is really only academic; at unity gain operation; however, the difference is a factor of 2.

CONSTRUCTION

The overall construction is relatively simple as can be seen in Figures 6 and 7. Copper-clad laminate was used for circuit wiring. Problems of ground loop pickup can be experienced if the power transformer is located anywhere near the low-level input leads. For this reason, the power supply and drive circuitry were located in a separate section. The dc supply leads and drive signal were then routed through feed-throughs. The 1000:1 divider is also located near the device sockets. For further general information on construction, the reader is referred to Motorola I/C Application Note AN-271.

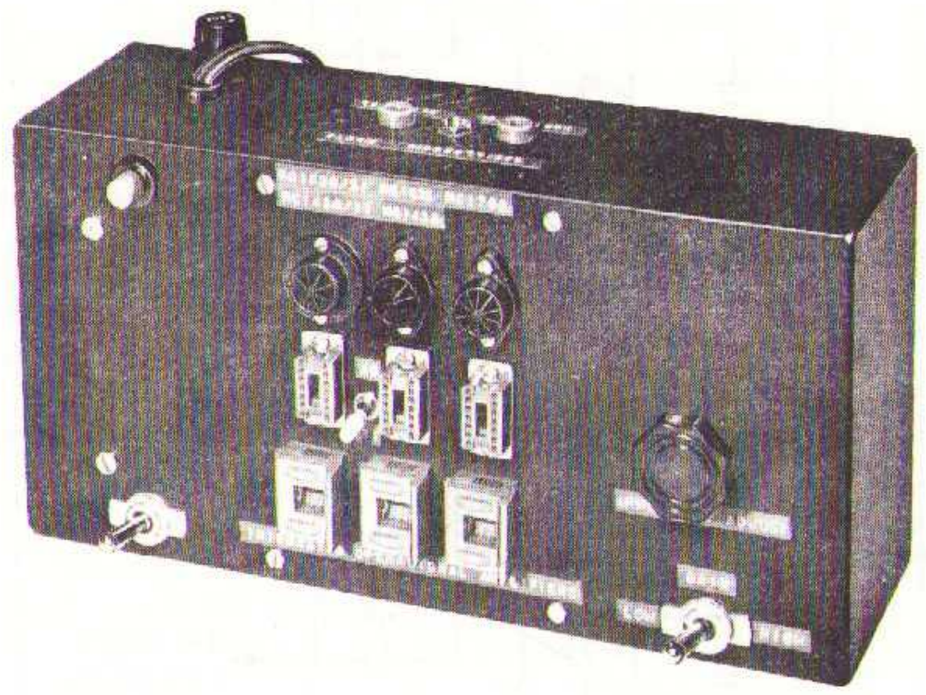

FIGURE 6 — TOP VIEW OF OPERATIONAL AMPLIFIER TESTER

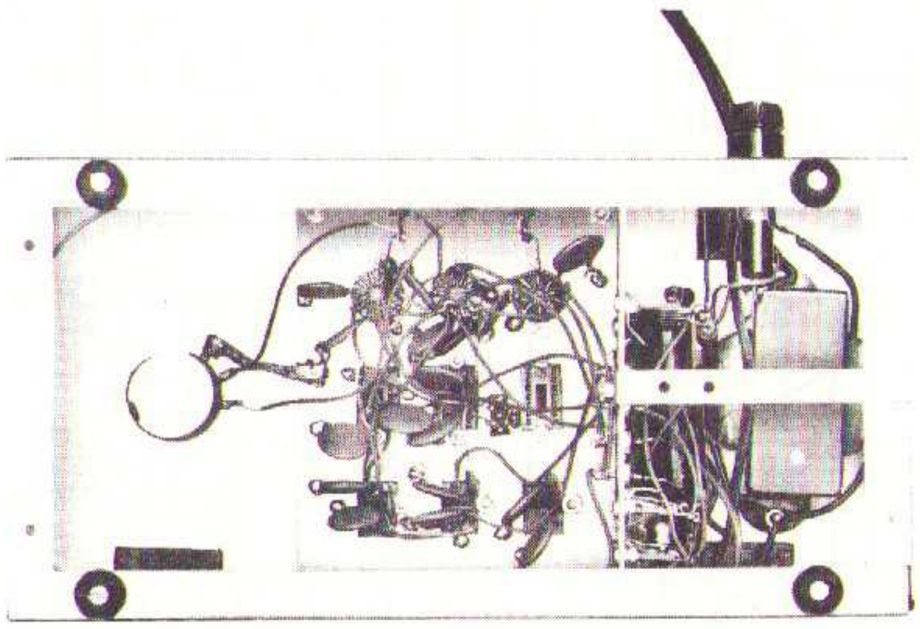

FIGURE 7 — BOTTOM VIEW OF OPERATIONAL AMPLIFIER TESTER

INTERPRETING THE OSCILLOSCOPE WAVEFORM

A typical transfer function is illustrated in Figure 8, with the main features noted.

Initially the oscilloscope inputs are grounded. The oscilloscope dot is then centered; this establishes the vertical and horizontal references. Insert the device to be tested into the appropriate socket. Turn up the amplitude adjust until the unit is in deep saturation. Read directly positive and negative $V_{o\ max}$. A_{VOL} is the calculated slope of the transfer function times 1000. V_{io} is the horizontal displacement from the horizontal reference to the point where the function crosses the vertical reference divided by 1000. The function through its transfer between the saturation points is also indicative of the device's linearity. In reading V_{io} and A_{VOL} from the scope presentation, it is advisable to increase the horizontal sensitivity so that the resolution is increased for better accuracy.

Keep in mind that if the oscilloscope voltage ranges are changed, it might be necessary to check the zero references; however, this is not necessary between checking different units.

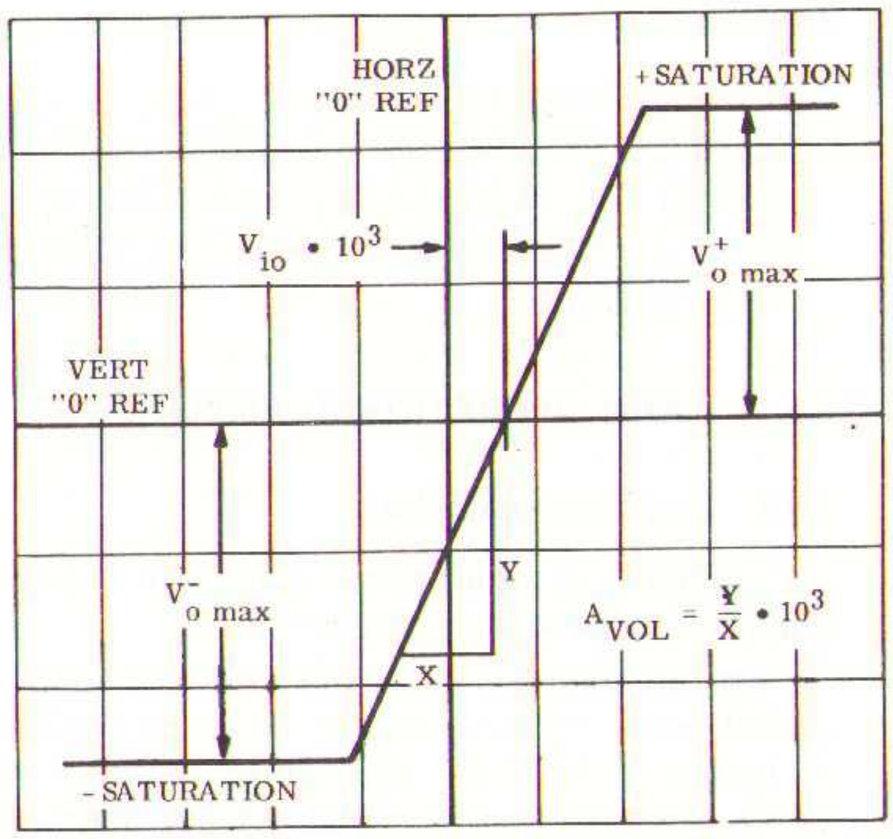

FIGURE 8 — TYPICAL OP-AMP TRANSFER CURVE

5. FREQUENCY COMPENSATION

5.1 GENERAL

Frequency compensation is both desirable and necessary for many applications of integrated circuits which have been designed with high internal voltage gains. Apart from stability considerations, frequency compensation may be used to greatly reduce broad-band noise caused by the integrated circuit itself (see appropriate Section) or fed in at the input, if the bandwidth required by the amplifier is small compared with the maximum bandwidth obtainable.

Application of negative feedback to a high-gain amplifier gives a circuit with characteristics dependent almost entirely on the feedback elements. The improvement in gain stability, phase shift, input impedance, output impedance and linearity is proportional to the amount of feedback. Thus, amplification to any degree of accuracy is possible with sufficient feedback. Large amounts of feedback, however, require that close attention be given to the amplifier open-loop characteristics. Stable circuits must have well defined open-loop gain and phase responses to frequencies far above the band of interest; 60 dB of feedback over a 10 kHz bandwidth, for example, requires controlled open-loop characteristics to over 10 MHz.

The frequency compensation networks required to stabilise the feedback amplifier depend on, among other things, the open-loop gain, the frequency response characteristics and the impedance at the compensation terminals of the amplifier. Specification of limits for each individual factor which affects the design of the frequency compensation networks will give an unnecessarily restrictive result, since variations in these factors correlate to some degree in an integrated circuit. It is better to treat the amplifier as a whole by specifying complete networks which guarantee stability for the full distribution of units.

The closed-loop gain of the simple amplifier shown in Fig. 5.1 is given by:

$$A_v = -\frac{A_{vo}}{1 + \beta A_{vo}} \qquad \ldots\ldots\ldots(1)$$

Where A_v = Closed-loop voltage gain
A_{vo} = Open-loop voltage gain
β = Feedback factor

The quantity $(1 + \beta A_{vo})$ is the amount of feedback and is a direct measure of the improvement obtained in performance of the amplifier. This factor must be greater than zero for all frequencies if the circuit is to be stable. Hence the magnitude of loop gain, βA_{vo}, must be less than unity at the frequency where the loop phase-shift is 180°. For realβ, the maximum amount of feedback is limited to the ratio of the low-frequency value of A_{vo} and the value of A_{vo} ot the 180° phase-shift frequency.

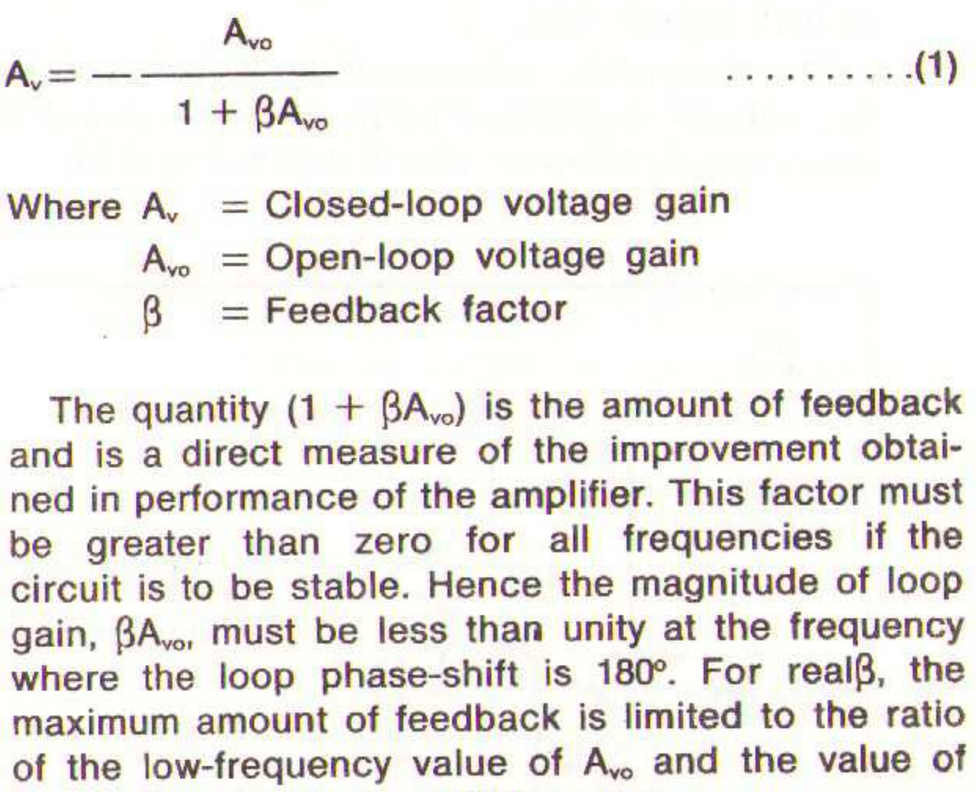

Fig. 5.1 - A Simple Feedback Amplifier

BIJ GEBRUIK VAN DE 741 OP AMP KOMEN DE HIER BESPROKEN FREQUENTIE-COMPENSATIES TE VERVALLEN. ZIE HIERVOOR HET IN DEZE DOCUMENTATIE OPGENOMEN DATASHEET.

5.3 μA709 OPERATIONAL AMPLIFIER

5.3.1 Lag Compensation

Practically all operational amplifiers require a frequency response compensation.

Two compensating points are provided in the μA709 element because of its high voltage gain; in fact it is normally difficult to obtain more than 60 dB attenuation with only one RC network.

The compensating points chosen feature a high internal resistance so that the amplifier can be compensated with small external capacitors.

The μA709 device cannot be used in open-loop configuration without any compensating network, because oscillations occur.

To avoid this drawback two capacitors are required: one $C_1 = 10$ pF between pins 1 and 8 and the other $C_2 = 3$ pF between pins 5 and 6 (Fig. 2.32 Section 2.5.3).

This is due to an internal feedback network (comprising R_7 and R_{15}) and to the difficulty of avoiding parasitic oscillations in amplifiers with a high gain at high frequencies.

The frequency compensation is obtained by an RC network connected between pins 1 and 8 and a capacitor C_2 between pins 5 and 6 (Fig. 5.21).

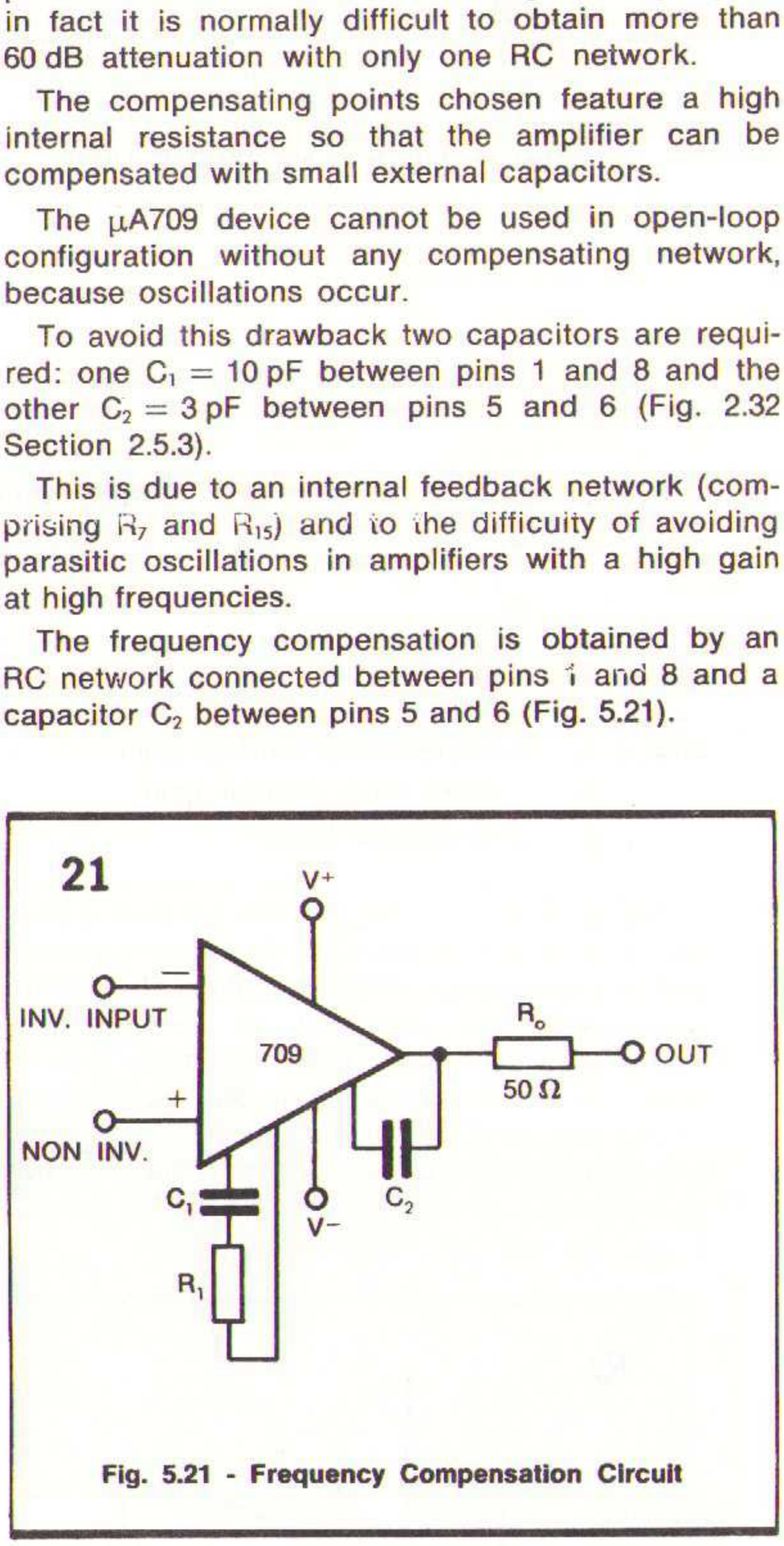

Fig. 5.21 - Frequency Compensation Circuit

Capacitor C_1 introduces a pole in the open-loop network at a frequency given by:

$$f_1 = \frac{1}{2\pi C_1 A_2 R_{i1}} \quad \ldots\ldots\ldots\ldots (1)$$

where:

R_{11} is the resistance between pin 1 and ground.

A_2 is the μA709 second stage voltage gain (TR_4, TR_6).

Resistor R_1 in series with capacitor C_1 introduces a zero at a frequency:

$$f_2 = \frac{1}{2\pi C_1 R_1} \quad \ldots\ldots\ldots (2)$$

Imiting the high-frequency attenuation introduced by the R_1 C_1 network at a value defined by:

$$A_C = \frac{R_{i1} A_2}{R_1} \quad \ldots\ldots\ldots\ldots (3)$$

The amount of such an attenuation is kept constant in different cases.

Finally, capacitor C_2 is chosen in order to introduce a pole at frequency f_2 such as to eliminate the effect of the zero introduced by resistor R_1 and to allow an open-loop response with an unity slope (20 dB/dec).

Hence:

$$C_2 = \frac{1}{2\pi f_2 R_{i5} A_4} \quad \ldots\ldots\ldots (4)$$

where:

R_{i5} is the resistance between pin 5 to ground.

A_4 is is the last-stage-but-one (TR_{12}) voltage gain.

The total attenuation introduced by the compensation networks has to be equal to the loop-gain, hence

$$\beta A_{vom} = A_c A_a \frac{f_a}{f_1} \quad \ldots\ldots\ldots\ldots (5)$$

where:

A_{vom} is the voltage gain with the source resistance R_S;

A_a is the attenuation due to the output compensating network;

f_a is the frequency which makes the loop-gain equal to 1.

At frequency f_a the amplifier has to show a phase margin enough to avoid oscillations or overshoots in the step response.

Solving the previous equations with respect to R_1, S_1 and C_2 we obtain:

$$C_1 = \frac{5 \cdot 10^{-8}}{1 + \frac{R_f}{R_s}} \ \mu F \qquad \ldots\ldots\ldots (6)$$

$$C_2 = \frac{2 \cdot 10^{-4}}{1 + \frac{R_f}{R_s}} \ \mu F \qquad \ldots\ldots\ldots (7)$$

$R_1 = 1.5\ k\Omega$

The amount of the attenuation A_c, which is constant for the different conditions, and hence the value of R_1, has been chosen in order that the frequency compensation does not appreciably affect the amplifier noise performance, and that capacitors C_1 and C_2 have roughly the same effect on the slewing rate.

Fig. 5.22 shows the small-signal open-loop gain for different values of the compensating network

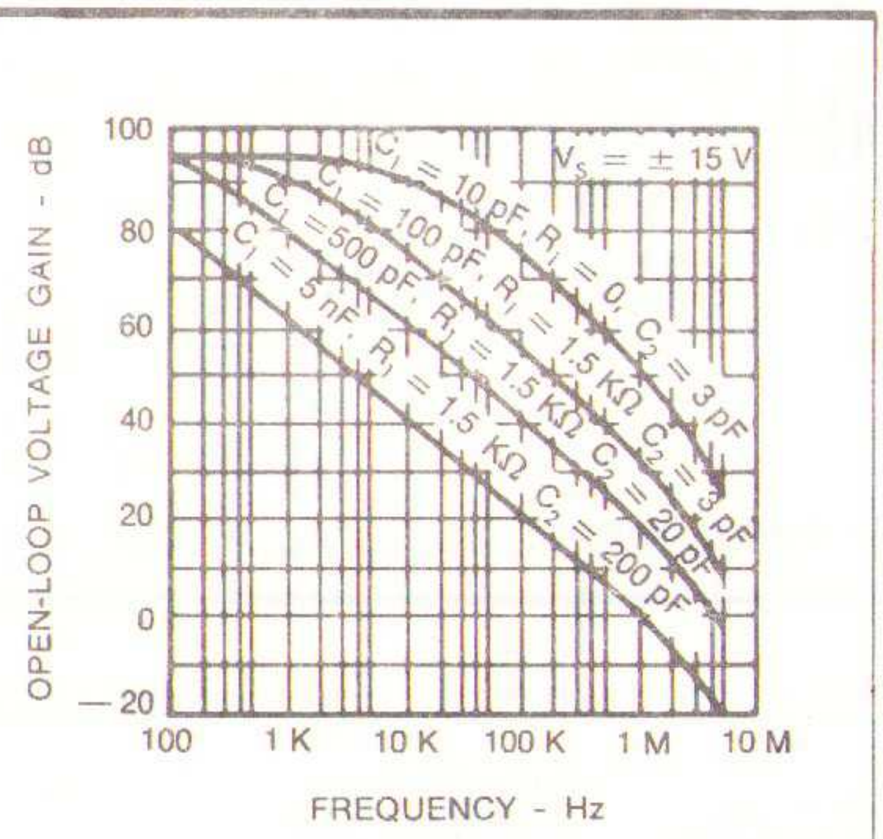

Fig. 5.22 - Open-Loop Frequency Response for Various Values of Compensation

It should be noted, that in presence of very small capacitive loads (50 pF - 100 pF) oscillations at very high frequency (10 - 15 MHz) often occur.

Such oscillations generally happen only when the NPN transistor TR_{14} is conducting.

These oscillations are due to the internal feedback provided by resistors R_7 and R_{15} and can be eliminated by connecting a 50 Ω resistor in series with the μA709 output: this sufficiently insulates such an amplifier from capacitive loads.

This resistor does not appreciably affect the integrated amplifier performance and introduces only a slight increase in output impedance (from 150 Ω to 200 Ω).

The frequency compensation described, is suitable in many respects: (small capacitance, values, independence from external resistance values, negligible influence in noise performance) but has the drawback of reducing the maximum output swing at high frequency.

Fig. 5.23 shows the maximum peak-to-peak voltage as a function of the frequency which can be obtained at the output for different values of compensation networks.

The slewing rate is about O.3 V/μsec. for a 20 dB/decade slope, over the unity gain point.

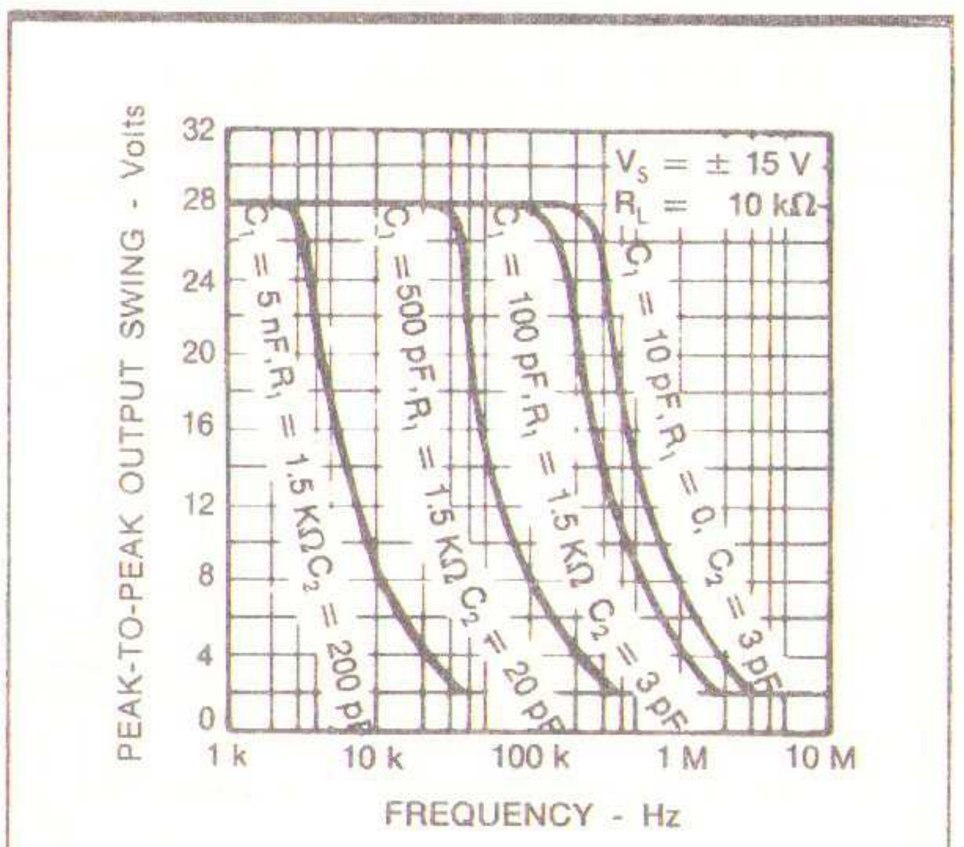

Fig. 5.23 - Output Voltage Swing as a Function of Frequency for Various Compensation Networks

5.3.2 Input Lag Compensation

In many applications, however, the reduction in output swing at high frequencies, due to the compensation already described, is unacceptable.

This limitation can be overcome using a compensation network, connected to the input pins, in addition to the ones connected between pins 1 and 8, 5 and 6, designed for the minimum values:

$C_1 = 10$ pF $\qquad R_1 = 0 \qquad C_2 = 3$ pF

The attenuation in the loop-gain introduced by the compensation network connected to the input pins, and comprising capacitor C_3 in series with the resistor R_3, is as follows:

$$A_c \cong \frac{2 R_s R_f}{(R_s + R_f) R_3} \qquad \ldots\ldots\ldots (8)$$

Hence from equations 5 and 8 we obtain:

$$R_3 = 2\,\frac{A_a}{A_o}\,R_f = 20\,R_f\ (\Omega) \qquad \ldots\ldots\ (9)$$

$$C_3 = \frac{A_o}{4f_a R_f} = \frac{9}{R_f}\ (\mu F) \qquad \ldots\ldots\ (10)$$

where R_f is expressed in kilohms.

5.3.3 Intermediate Frequency Compensation

The input compensation, even though it improves the intrinsic slewing rate characteristic of the device, causes a worsening of the amplifier noise performance; which is considerable when the closed-loop gain approaches unity.

This is the reason why, in many cases, the use of compensation, which is a compromise between noise and slewing rate performance, is preferred.

A simple way to design the new networks is to choose C_1 and C_2 to obtain the required slewing rate: the necessary attenuation and stability with frequency being obtained by use of the network connected to the input.

Equation (8) gives the design criteria for the value of R_3 while the value of C_3 can be obtained from (10).

The amount of attenuation introduced by the RC network connected to the input indicates how the noise performance deteriorates.

Table 2 shows the experimental results of the unity-gain inverter amplifier shown in Fig. 5.24, for all the aforementioned configurations.

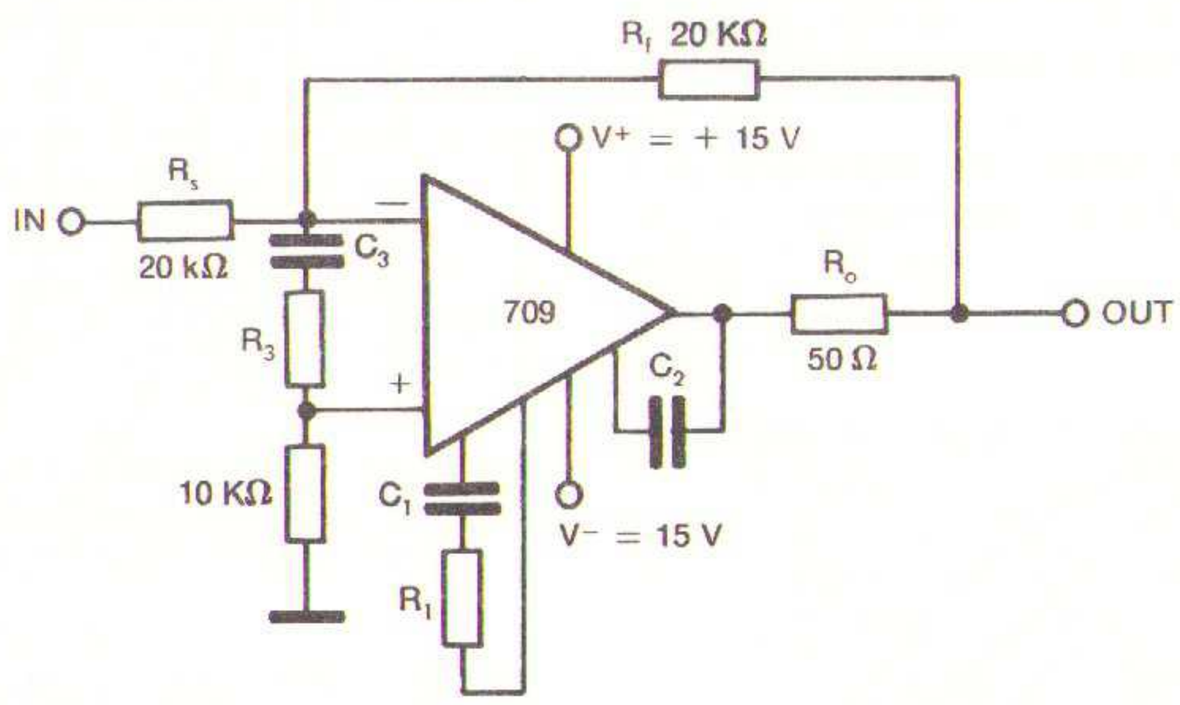

Fig. 5.24 - Unity Gain Inverting Amplifier

Kind of compensation	LAG COMPENSATION	INPUT LAG COMPENSATION	INTERMEDIATE FREQUENCY UNIT COMPENSATION	
	$R_1 = 1.5\ k\Omega$ $C_1 = 5000\ pF$ $C_2 = 200\ pF$	$R_3 = 39\ \Omega$ $C_3 = 0.47\ \mu F$ $C_1 = 10\ pF$ $C_2 = 3\ pF$ $R_1 = 0$	$C_3 = 0.47\ \mu F$ $R_3 = 1\ k\Omega$ $C_1 = 250\ pF$ $R_1 = 1.5\ k\Omega$ $C_2 = 10\ pF$	
Bandwidth (— 3 dB)	500	500	500	KHz
Full power response	4.5	300	80	KHz
Slewing Rate	0.3	22	6	V/μsec.
Noise Voltage	0.03	20	1.3	mVp-p.

Table 2

5.3.4 Frequency Response with a Slope Higher than 20 dB/dec.

In the preceding paragraphs, amplifiers having a unity slope (20 dB/dec.) frequency response have been considered, because the ones with a greater slope are, at first sight, more difficult to stabilize even if they offer some advantages with respect to conventional amplifiers.

The stabilization difficulties can be easily overcome with amplifiers having a frequency response slope of 40 dB/dec. for high gain values ($\geq$40 dB), and a slope of 20 dB/dec. near the unity gain.

Fig. 5.25 shows the frequency response in both cases for the μA709 device, and the component values of the compensation networks.

It is evident that the amplifier with a slope greater than 20 dB/dec. has a higher open-loop gain at low frequencies.

Consequently in this region the amount of negative feedback is greater and hence it is possible to have higher closed loop-gain stability, lower distortion and a smaller output impedance.

The compensation capacitors are smaller, and this means shorter recovery times and reduced overall dimensions, therefore these amplifiers can exhibit higher slewing rates and better noise performance.

There are no problems concerning stability with frequency when the closed-loop gain is approximately unity, but there are overshoots in presence of step functions, and oscillations with higher gains.

These oscillations can, however, be eliminated by a small capacitor C_7 connected in parallel with the feedback resistor.

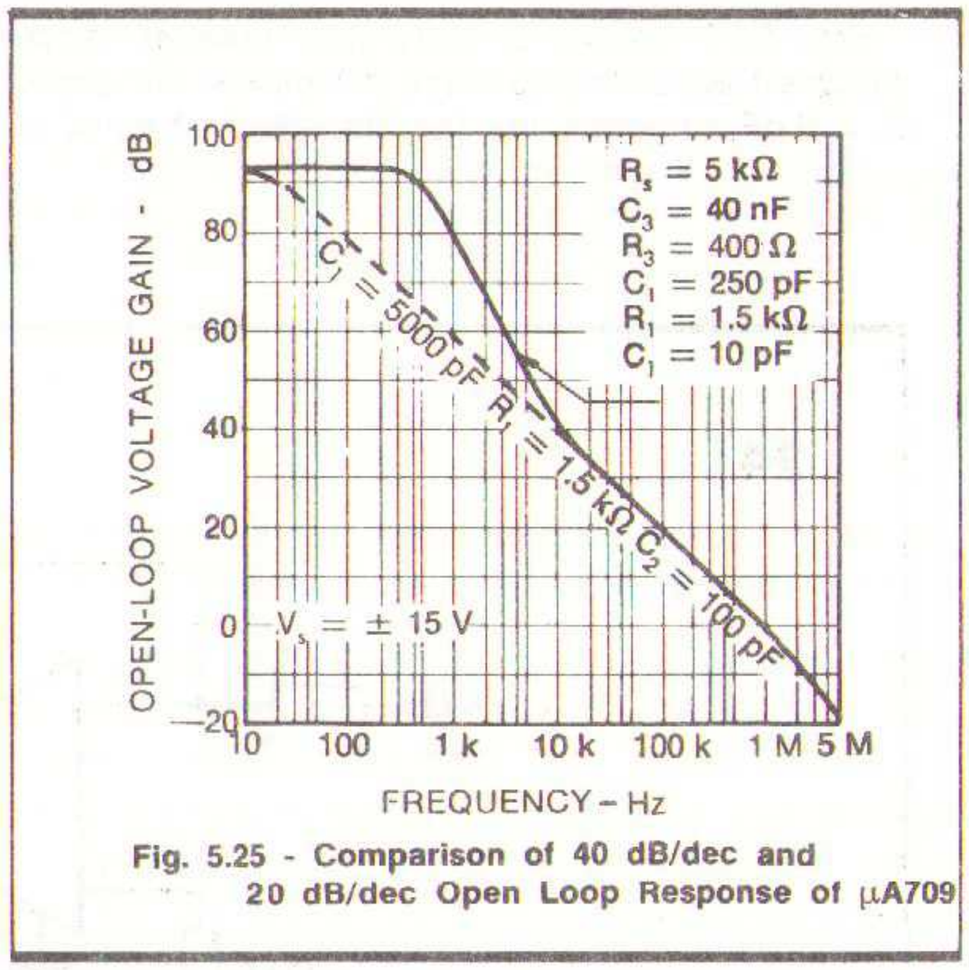

Fig. 5.25 - Comparison of 40 dB/dec and 20 dB/dec Open Loop Response of μA709

maintenance of stability allowing for the 'spread' of parameters during manufacture of the semiconductors.

In some cases it might be convenient to use systems whose performance is not so exacting in order to achieve a larger bandwidth.

This is obtained, for instance, using the compensation shown in Fig. 5.26 (a) which differs from the one described in Section 5.3.1 because a resistor R_2 has been connected in series with the capacitor C_2 in order to compensate for the second pole which appears in the open-loop frequency response of Fig. 5.22.

Fig. 5.26 (b) shows the open-loop frequency response with such a compensation; it is evident that the improvement in both bandwidth and slewing rate characteristics by almost a factor of 5, in conjuction with a higher capacitive-load-sensitivity, is obtained.

5.3.5 Other Circuits

The design criteria for the compensation network described in the preceding paragraphs ensure the

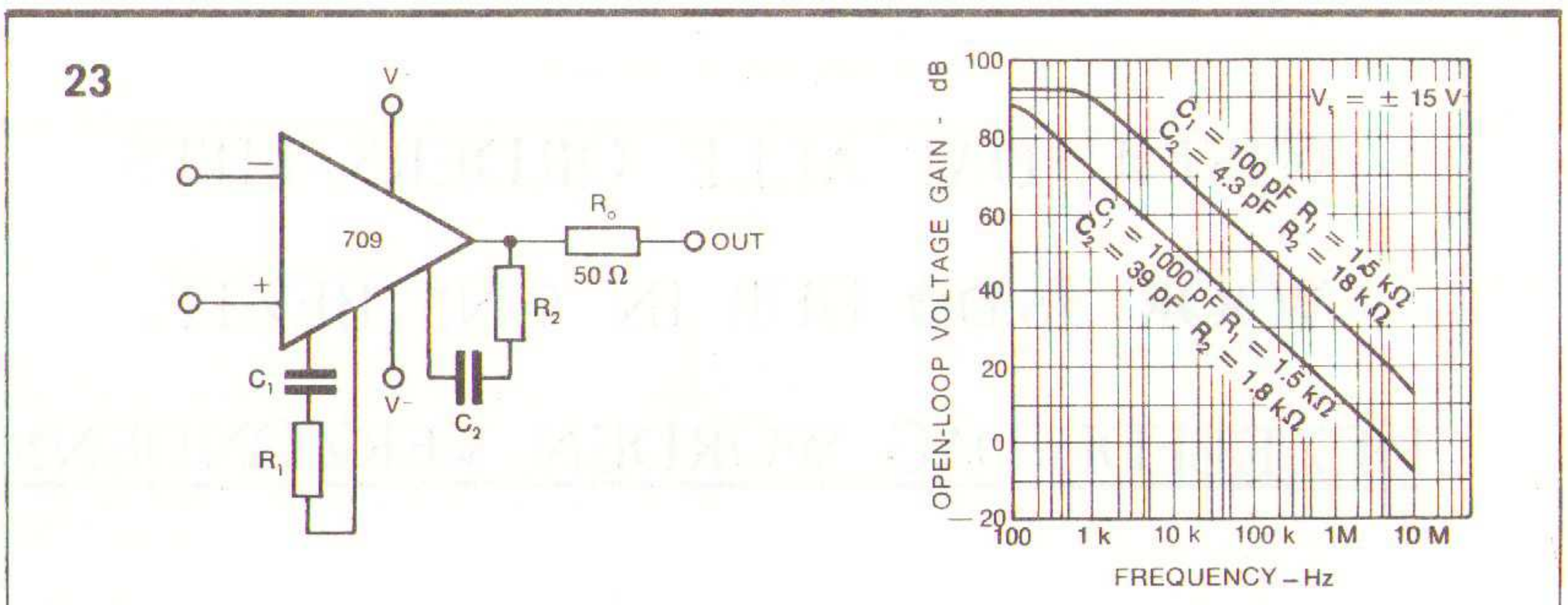

Fig. 5.26 - Frequency Compensation Circuit for Wider Band and Open Loop Voltage Response

Fig. 5.27 shows a unity-gain inverter amplifier designed according to these principles: the capacitor $C_f = 3$ pF compensates for the effect of input capacitance. It feaures a bandwidth of about 2 MHz, a full-power response up to 20 KHz and slewing rate of 1.5 V/μsec.

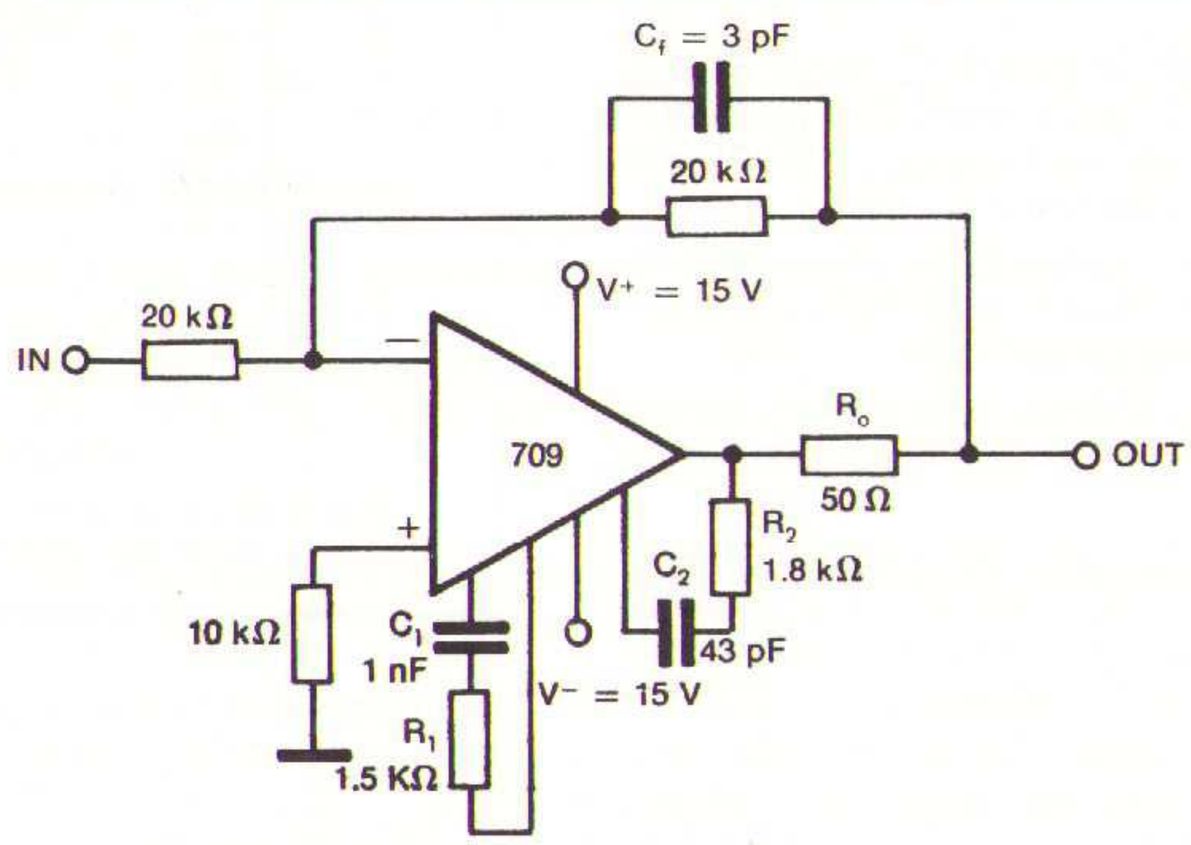

Fig. 5.27 - Wideband Unity Gain Inverting Amplifier

3.3 709 BASIC AMPLIFIER CIRCUITS

3.3.1 Inverting Amplifier

Fig. 3.30 shows the amplifier circuit diagram of an inverting amplifier using the μA709 where the output voltage is input voltage dependent as shown by the following formula:

$$e_o = -\frac{R_2}{R_1} e_1$$

In this circuit the output impedance of the amplifier is reduced by means of feedback to values less than one ohm while the input impedance is:

$$Z_{in} = \frac{e_{in}}{I_{in}} = R_1$$

The stability versus frequency is obtained by R_4, C_1, C_2 groups designed to obtain the maximum bandwidth (0.5 MHz).

The circuit can obviously also operate with different resistance values and, in consequence, with different closed-loop gains.

It should be ncted that offset noise and thermal drift indicate the minimum applicable signal, while the input current, noise current and bandwidth requirement limit the maximum resistances values.

25

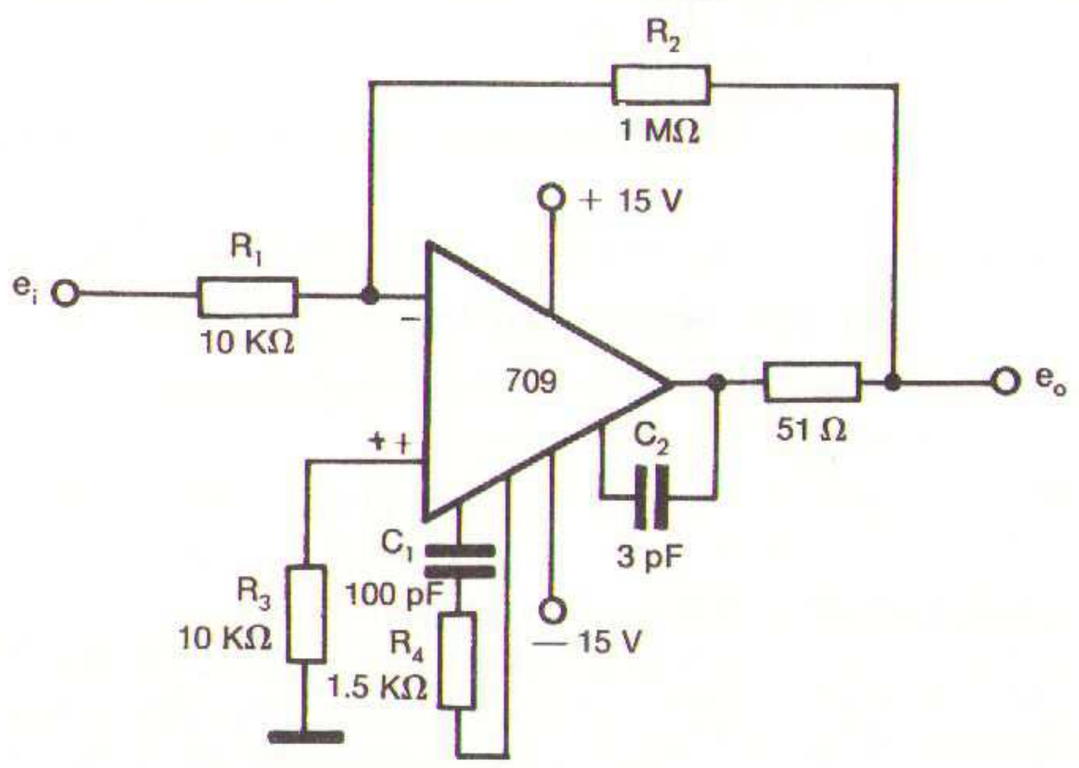

Fig. 3.30 - Inverting Amplifier

3.3.2 Non-Inverting Amplifier

The excellent differential characteristics, the high gain and high input voltage range of the μA709 make this device particularly suitable for non-inverting amplifier applications.

Fig. 3.31 shows an amplifier of this type made with the μA709 device whose gain is defined by the following equation:

$$e_o = \frac{R_1 + R_2}{R_1} e_1$$

The output impedance is lowered up to values of a fraction of an ohm by negative feedback, while the input impedance rises, as given by:

$$Z_{in} = \frac{1}{Y_{in}} = \frac{1}{Y_{3G} + Y_{23} \dfrac{1}{1 + \dfrac{A_o}{\dfrac{R_1 + R_2}{R_1}}}}$$

where Y_{3G} and Y_{23} are the admittances between input + and ground and inputs − and + respectively. Since the μA709 common admittance ($Y_{3G} = Y_{G2}$) is very low at low frequency, of the order of $10^{-8}\Omega^{-1}$ the input resistance is given by:

$$R_{in} = \frac{1}{Y_{23}} \left(\frac{R_1}{R_1 + R_2} A_o \right)$$

Finally, the compensation network has been designed to obtain the maximum bandwidth, while the resistance R_s has been chosen equal to $R_1 // R_2$ to minimise offset and drift.

26

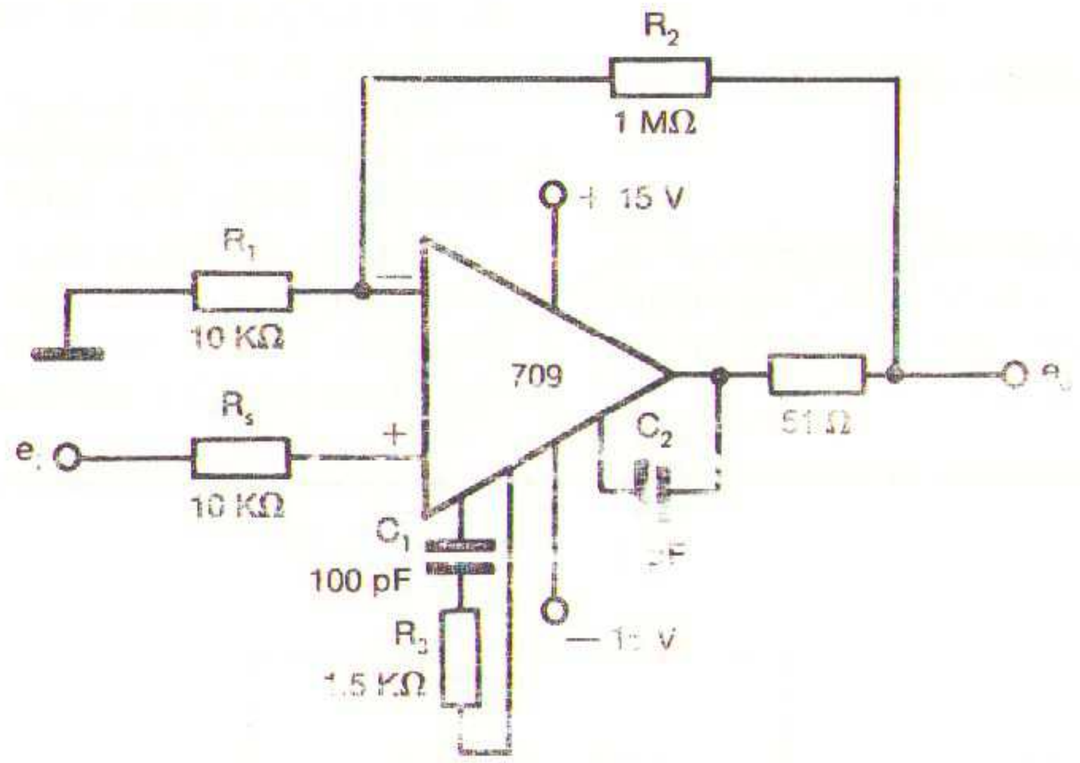

Fig. 3.31 - Non-inverting Amplifier

3.3.3 Differentiator

Fig. 3.32 (a) shows the circuit diagram of a differentiator using the μA709 element.

The current flowing into the summing point through the capacitor C_d is defined by the equation:

$$i_c = C_d \frac{de_i}{dt}$$

Since the current i_c is equal to the feedback current flowing through resistor R_d (less the μA709 input current) the output voltage is given by:

$$e_o = -i_c R_d = -R_d C_d \frac{de_i}{dt} = -T_d p e_i$$

The circuit diagram shown in Fig. 3.32 (a) differs from the ideal differentiator by the addition of capacitor C_r and resistor R_i.

These components have been added to ensure the necessary frequency response stability to the differentiator circuit. More-over, limiting the gain measured at high frequencies obviously higher than the operating [illegible] noise can be drastically reduced.

Resistor R_i is inserted to [illegible] across capacitor C_d, thus avoiding source overloads.

In addition, the circuit acts as a differentiator at low frequencies, an integrator at high frequencies and as a proportional amplifier at intermediate frequencies as indicated in Fig. 3.32 (b).

The differentiator time-constant is selected so that the maximum rate of change of input signal will produce full-scale output not higher than the maximum allowable e_{omax}:

$$R_d C_d = \frac{e_{omax}}{\left| \frac{de_i}{dt} \right|_{max}}$$

Finally, the error produced by summing point voltage and current offset referred to the input is:

$$\left(\frac{de_i}{dt} \right) \text{error} = \frac{1}{C_d} \left(\frac{1}{R_d} e_{offset} + I_{offset} \right)$$

27

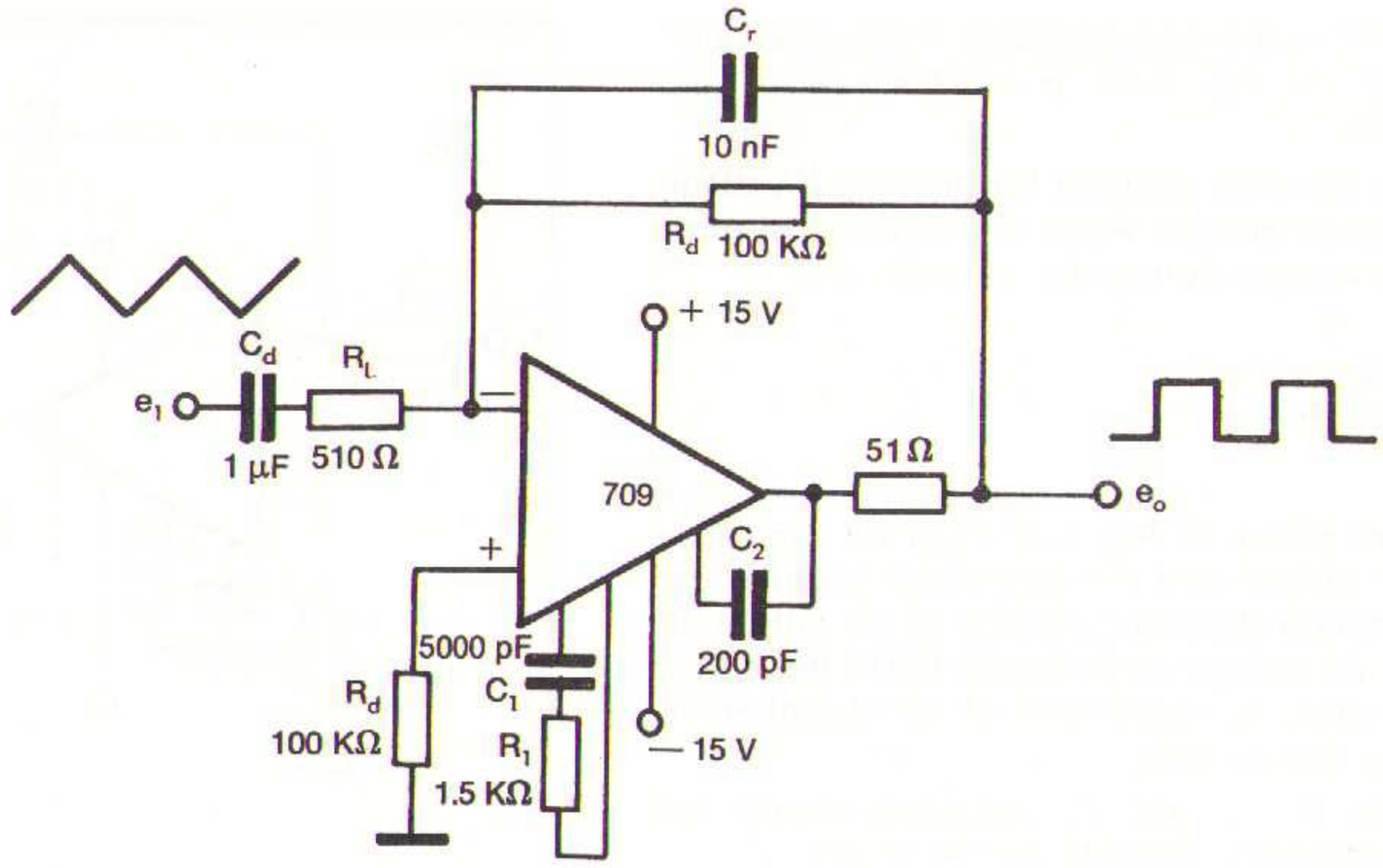

Fig. 3.32 (a) - Practical Differentiator

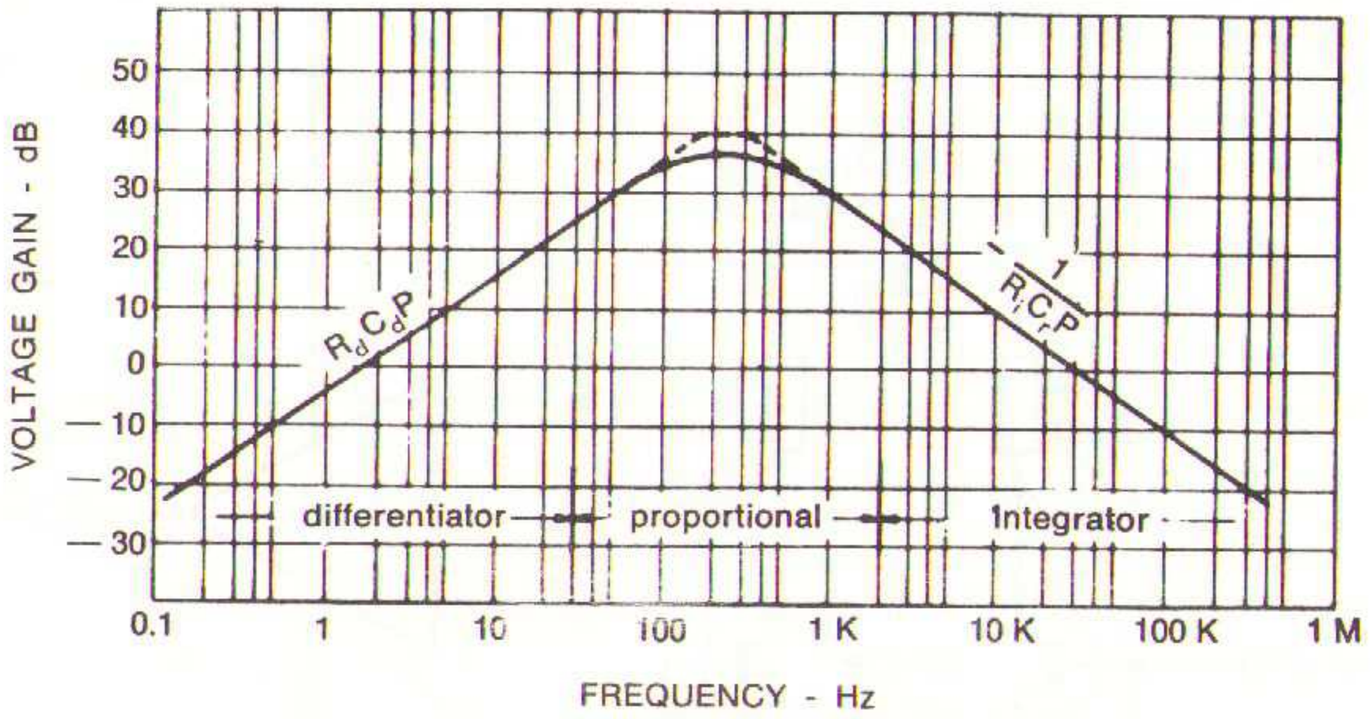

Fig. 3.32 (b) - Frequency response of pratical differentiator of fig. 3.32 (a)

3.3.4 Integrator

The capability of being able to execute the integral operation accurately is of fundamental importance in many applications.

The circuit in Fig. 3.33 shows a free-running integrator (i.e. without reset or hold circuits) made with a µA709 element.

Since the current e_1/R flowing across the input resistor must pass through the feedback capacitor, we obtain:

$$-C\frac{de_o}{dt} = \frac{e_1}{R}$$

and thus:

$$e_o = -\frac{1}{R_c}\int^{t} e_1 dt = -\frac{e_1}{pT}$$

where T = RC is the time-constant of the integrator. For example, in Fig. 3.33, R = 100 kΩ, C = 1 μF, RC = 0.1 sec.

T is really the time required for the output voltage to change by an amount equal to the average value of the input voltage during the time Δt:

$$-\Delta e_o = \frac{\Delta t}{T}\overline{e_i}$$

The circuit shown in Fig. 3.33 must be used in a closed-loop system and equipped with circuits capable of setting a starting condition at the output; in fact, due to its voltage and current offset the actual integration tends to reach one of its saturation limits within a certain time.

Finally, the R_1, C_1 and C_2 networks ensure the necessary frequency stability at the output.

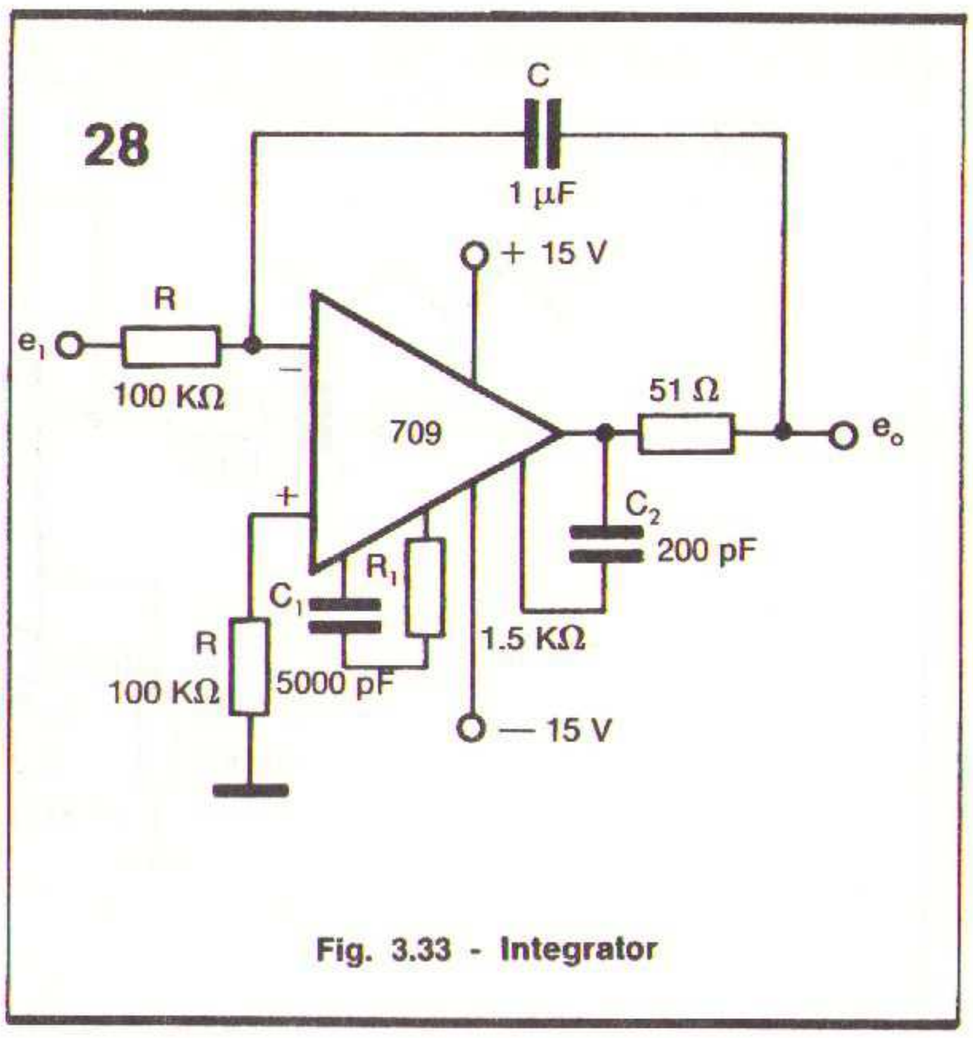

Fig. 3.33 - Integrator

3.3.5 Low Input Current D.C. Amplifier

In spite of the excellent input characteristics of the μA709 operational amplifier there are applications where better performances are required.

For instance, in logarithmic amplifiers with a higher swing than the one described in Section 3.4.5,

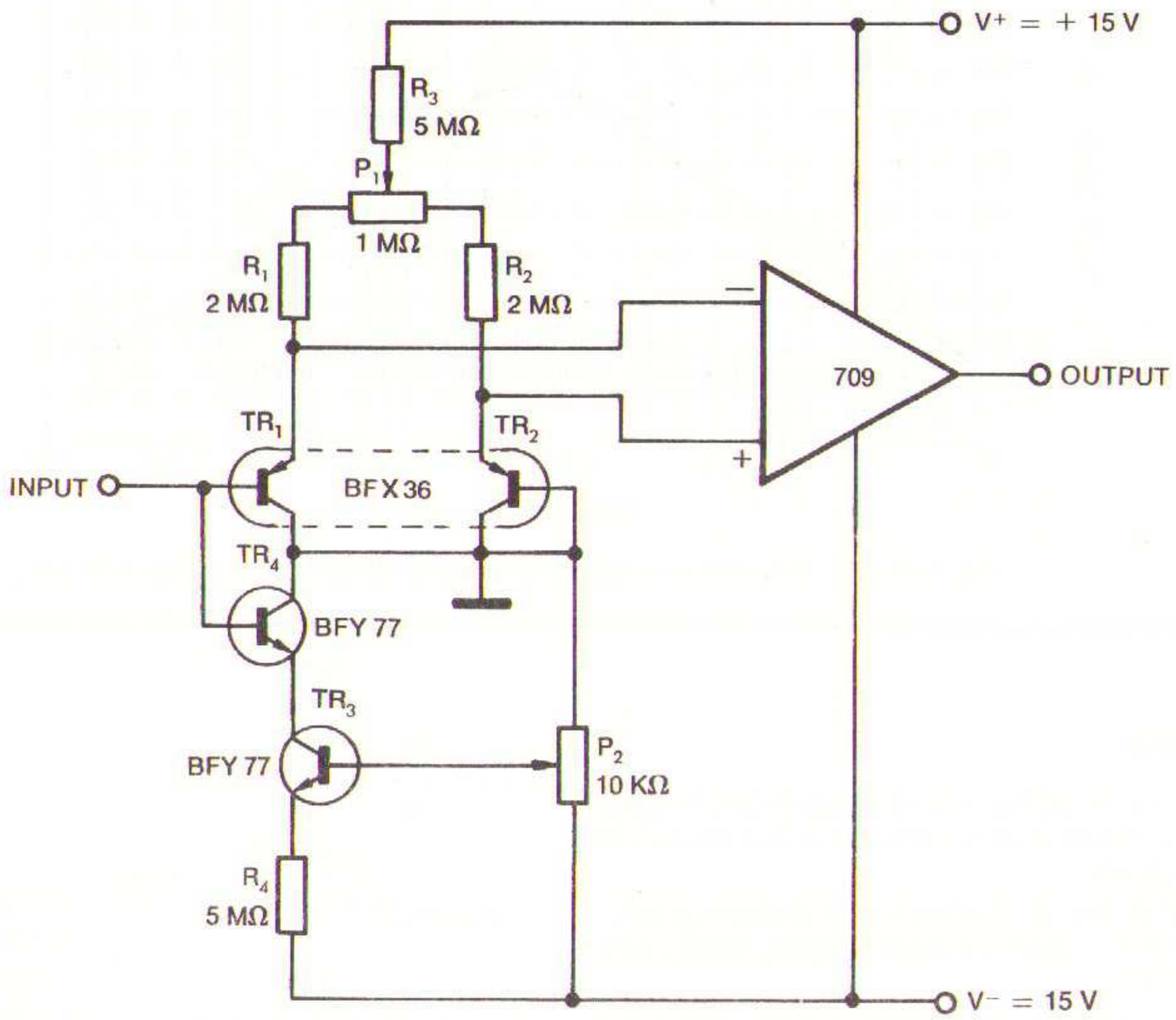

Fig. 3.34 - Low Input Current D.C. Amplifier

in summing amplifiers with high values of source resistance and in high-linearity and large time-constant integrators there is the need for improved input characteristics.

Fig. 3.34 shows the operational amplifier circuit diagram employing a μA709 element and a differential stage in a common-collector configuration, with a dual PNP transistor type BFX36.

In this amplifier the voltage drift is equal to the sum of the μA709 voltage drift and that of the input stage added to the μA709 current drift multiplied by the output impedance of the common-collector stage.

The adaptor stage operates with a very low collector current (1μA) and practically zero collector-base voltage.

This is the reason why the influence of the I_{CBO} of the transistors is eliminated, and the current drift is due to current gain variations with temperature.

The amplifier has a high input impedance (15 MΩ) and a small input current (5-10 nA).

The input current at ambient temperature can become zero by the current generator comprising TR_3 and transistor TR_4 which are complementary to TR_1: in fact by adjusting potentiometer P_2 it is possible to alter the current of TR_3 and consequently that of TR_4 in order that:

$I_{b4} = \frac{I_{C4}}{h_{FE4}}$ be equal to the base current

or TR_1 which is $I_{b1} = \frac{I_{C1}}{h_{FE1}}$

Moreover it is possible to obtain a current drift improvement within a limited temperature range (O to 60°C); in fact a typical current drift value is 20 pA/°C.

An improved increase in D.C. stability is obtained by keeping the temperature of the whole amplifier constant, this is possible due to its small dimensions. Note (1). Potentiometer P_1 is used to adjust the voltage offset with the input short-circuited to ground.

3.3.6 Power Booster Amplifier

The output power of the μA709 operational amplifier is satisfactory for most applications but insufficient to drive resistive and capacitive loads requiring more than a few milliamperes.

Greater output power may be obtained by adding a unity voltage gain power booster, in cascade with the integrated amplifier — within the feedback loop.

Fig. 3.35 (a) shows the block schematic of the complete amplifier when the booster is connected as the output stage of the μA709, all the supply decoupling components are shown, together with suitable compensating networks for the amplifier.

The integrated amplifier determines the input conditions, bandwidth and slewing rate while the output characteristics derive from the booster.

Fig. 3.35 (b) shows the power booster circuit. Two difectly-coupled voltage amplifier stages in cascade drive the complementary output stage. The output is connected back to the emitter of the first stage, and gives 100% negative feedbak to maintain the voltage gain at unity, increases the input impedance and improves the bandwidth.

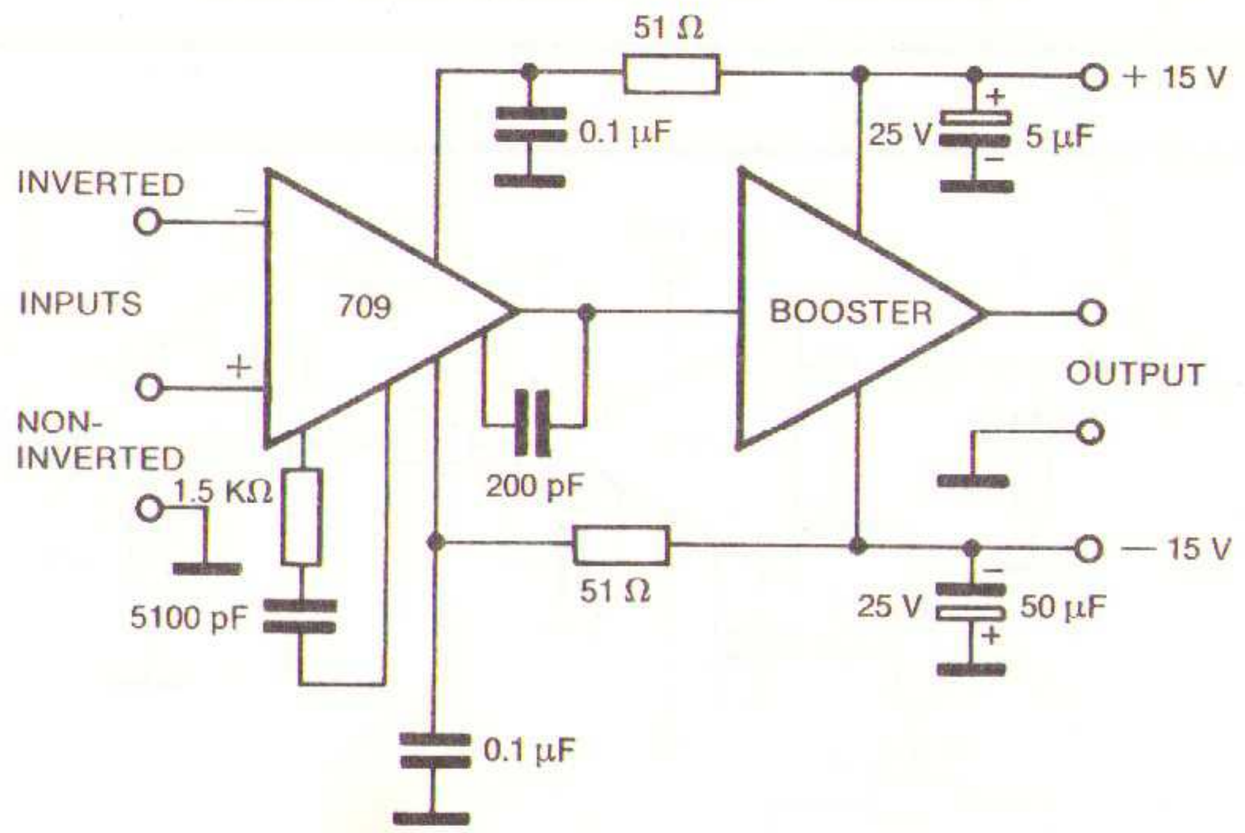

Fig. 3.35 (a) - Block Schematic of Operational Amplifier and Power Booster

The booster under consideration, protected up to a maximum ambient temperature of 50°C, against a permanently short-circuited output for all input signals, allows an output voltage swing of ± 10 V to be obtained with a load of 100 Ω.

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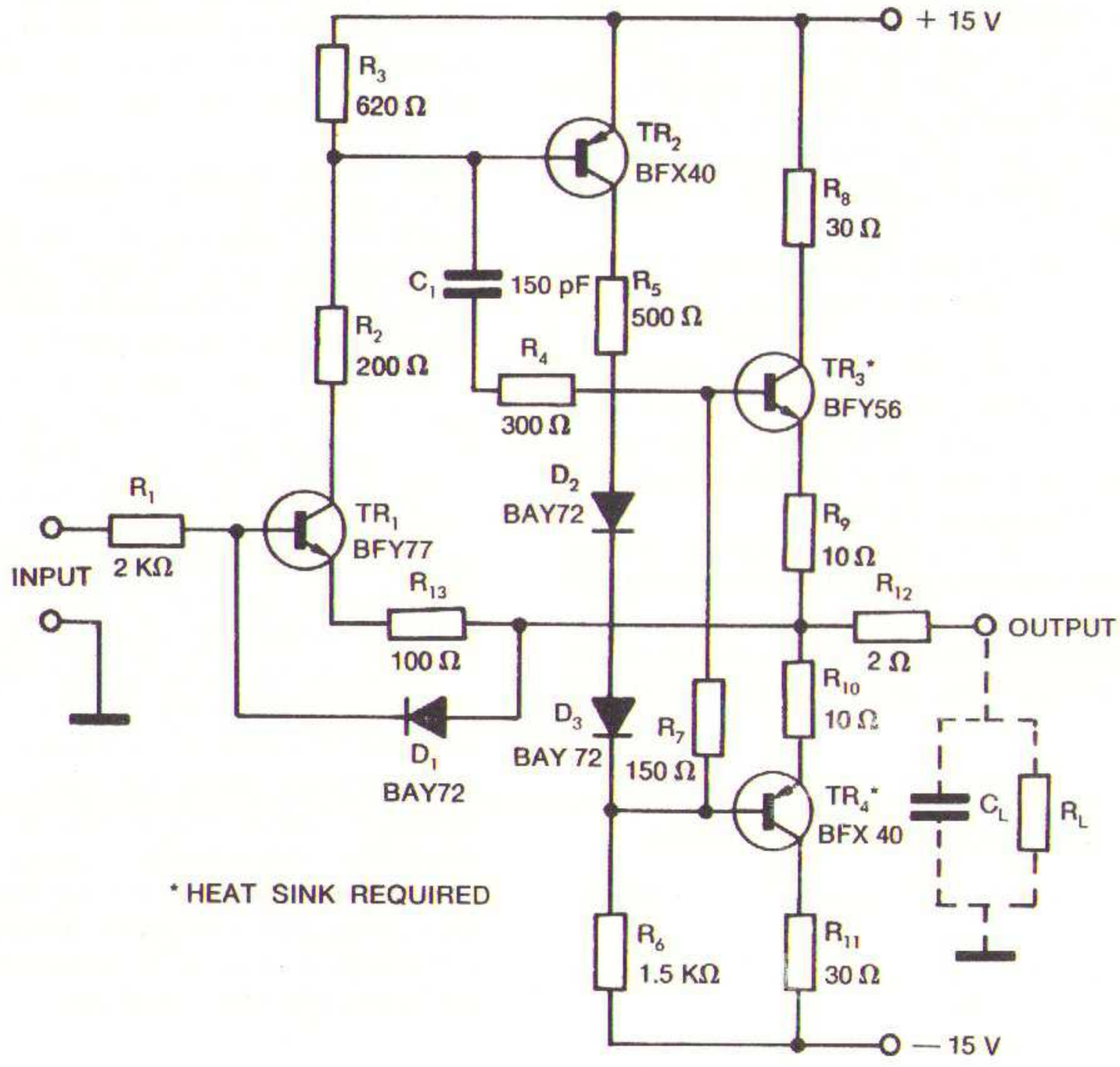

Fig. 3.35 (b) - The Power Booster Circuit Diagram

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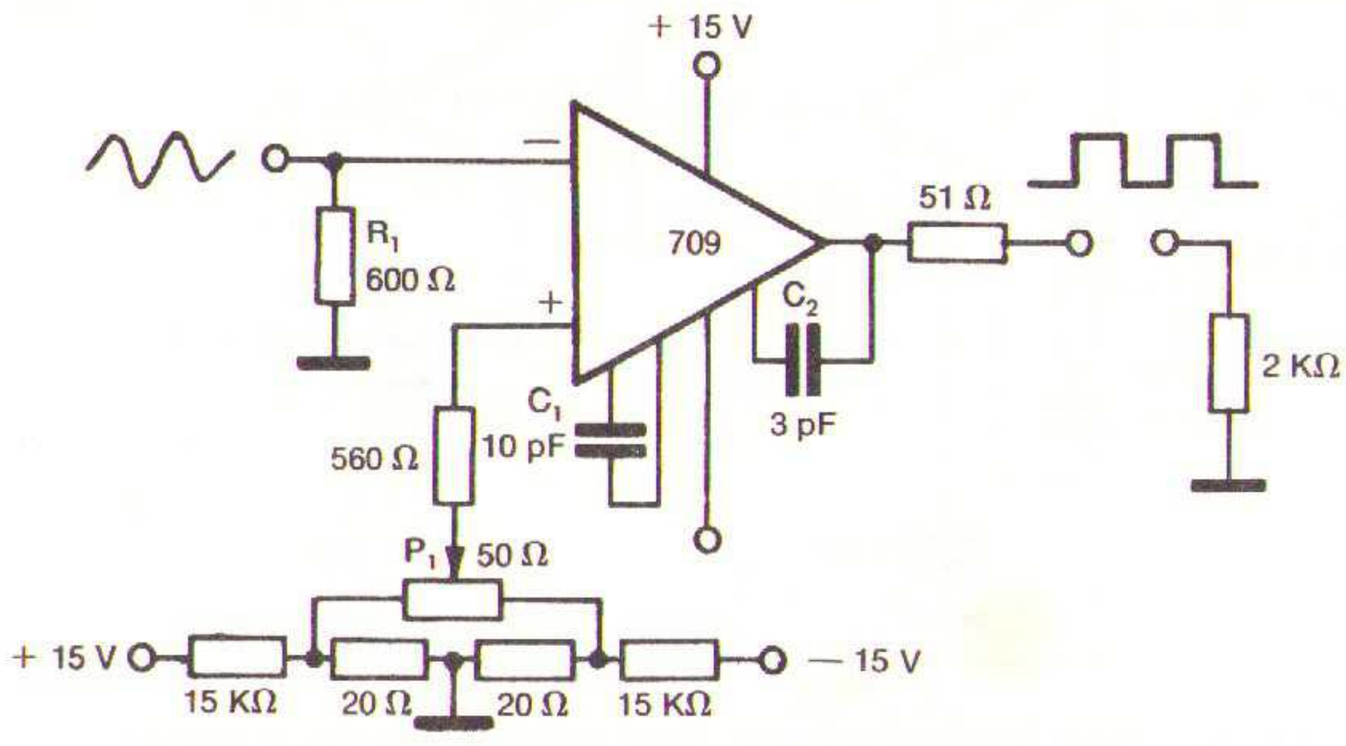


Fig. 3.36 (a) - Squarer

3.4 MISCELLANEOUS CIRCUITS

3.4.1 Squarer

Fig. 3.36 (a) shows a low-frequency squared using the high performance μA709 element.

The input impedance is governed, to within a few percent, by the resistor R_1 in parallel with the non-inverting input since the input intrinsic resistance of the μA709 remains fairly high at each operating condition.

The maximum input level is limited at ± 5 V zero-to-peak (= + 13 dBm) by the breakdown voltages of the input transistor base-emitter junctions.

Fig. 3.36 (b) shows the limiting characteristic with a sinusoidal input signal at a frequency of 1 KHz where the output voltage has been measured with a true root-mean-square voltmeter.

Potentiometer P_1 is used to adjust the offset voltage to zero and to produce a symmetrical square-wave at the output, with the minimum input signal (— 55 dBm).

Under such conditions the squarer can operate for signals between — 55 dBm and + 10 dBm, keeping the square wave at the output symmetrical to within 1% accuracy.

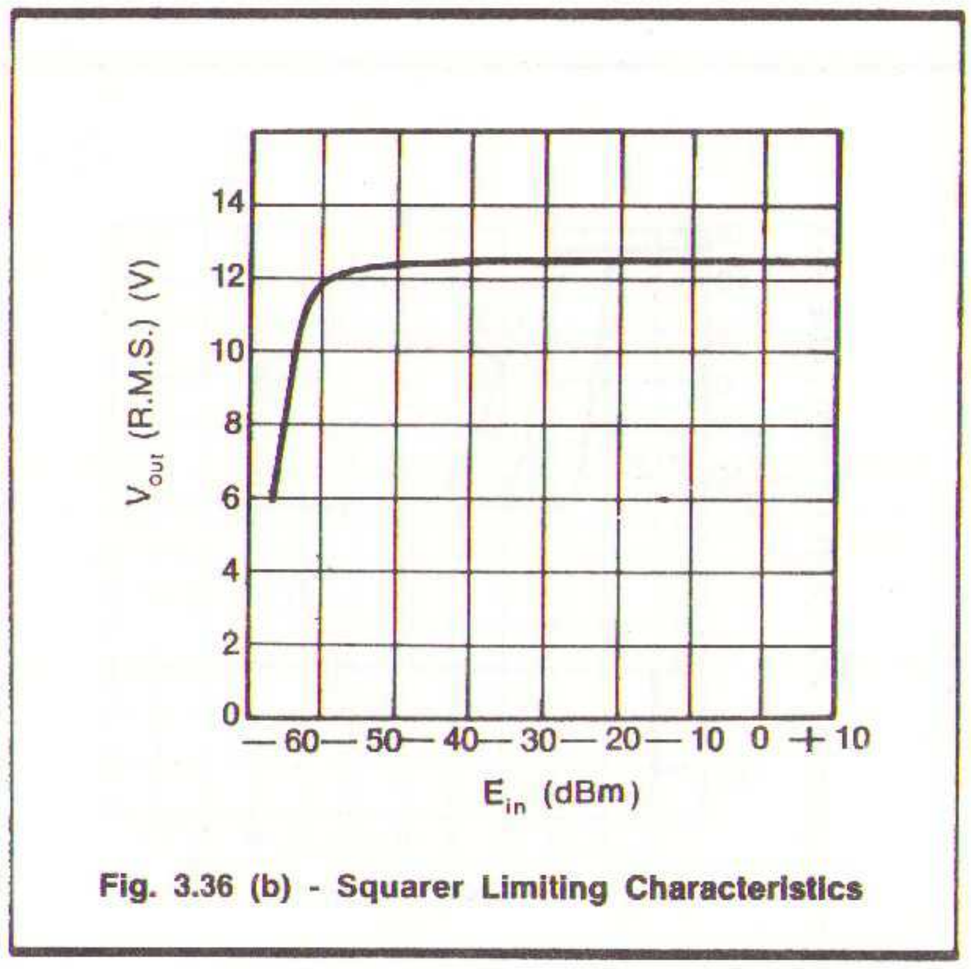


Fig. 3.36 (b) - Squarer Limiting Characteristics

3.4.2 Comparator

The μA709 integrated amplifier can be used as voltage comparator, particularly at low frequency, as shown Fig. 3.37 (a). The reference and input voltages must not exceed the maximum allowable limits for both common and differential signals which can be applied to the input.

The integrated amplifier is used in open-loop configuration with the compensating networks designed for the minimum values.

The input-output transfer function is shown in Fig. 3.37 (b); note the low transition voltage.

The curve corresponds to the condition in which the offset voltage has been set to zero, otherwise the transfer function will remain within the limits of ± 5 mV of the input voltage.

Since voltage comparators are often used to measure the difference between a square wave and the reference voltage, switching times are important.

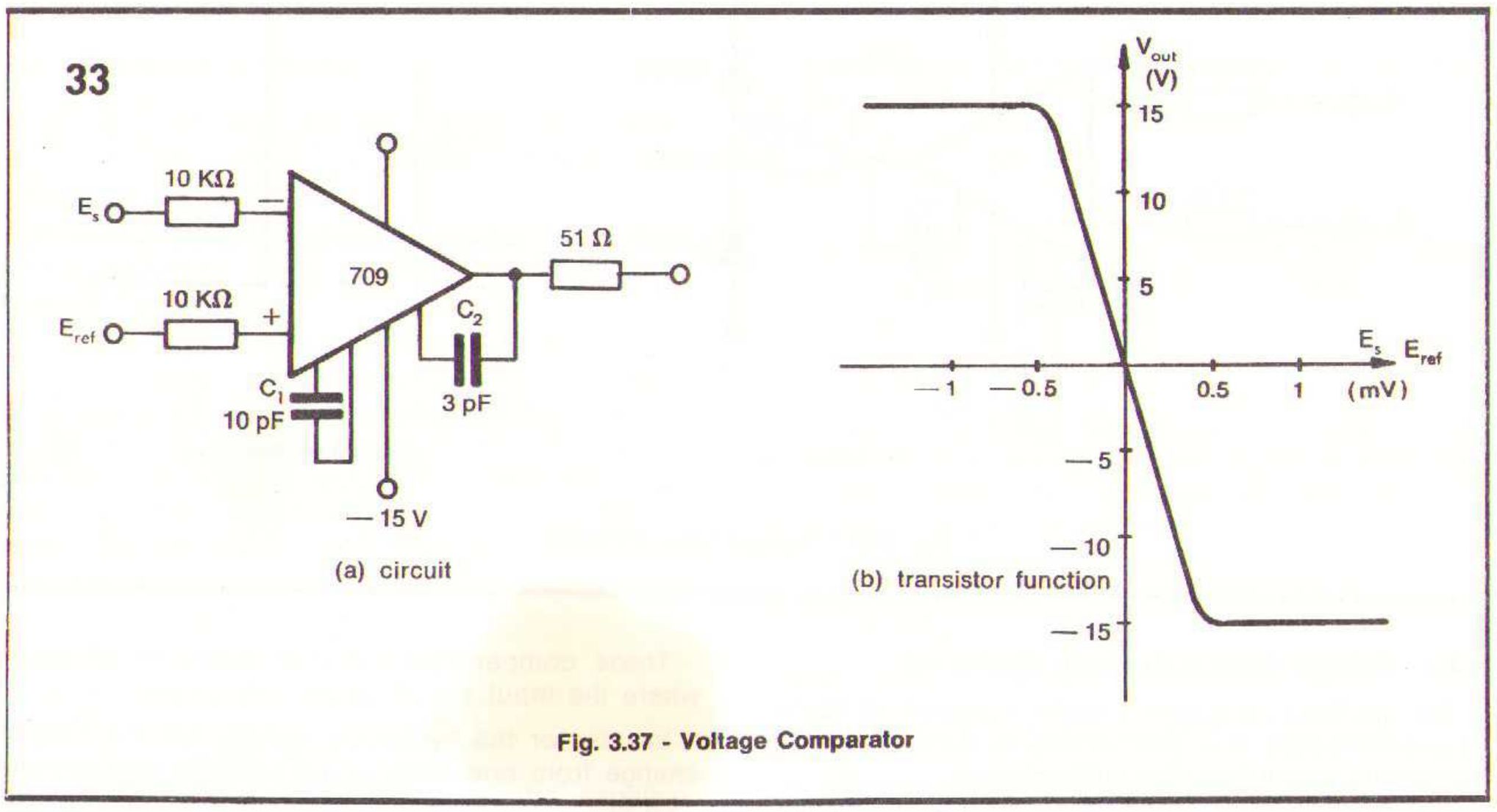


Fig. 3.37 - Voltage Comparator

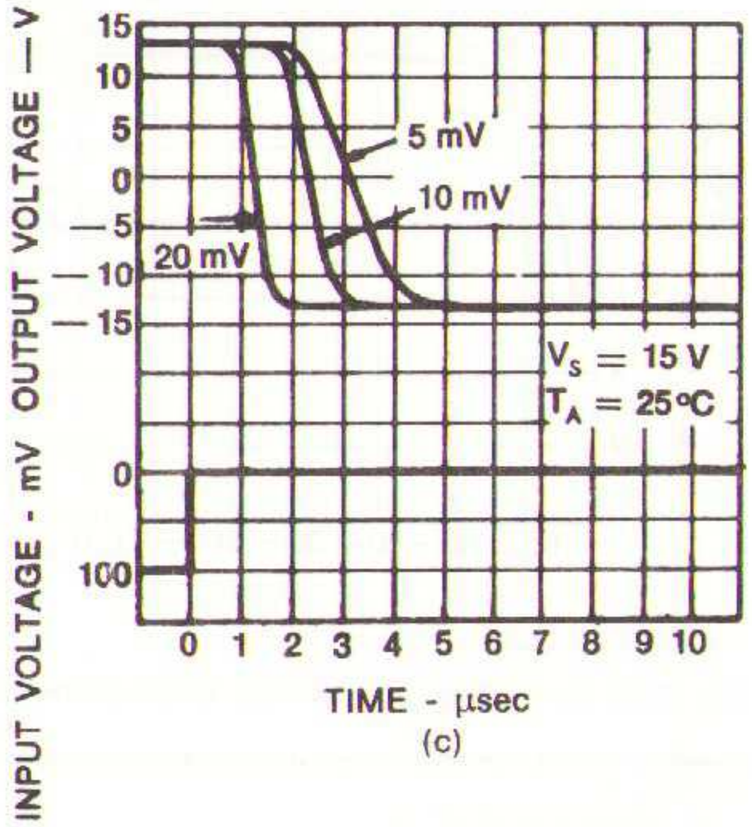
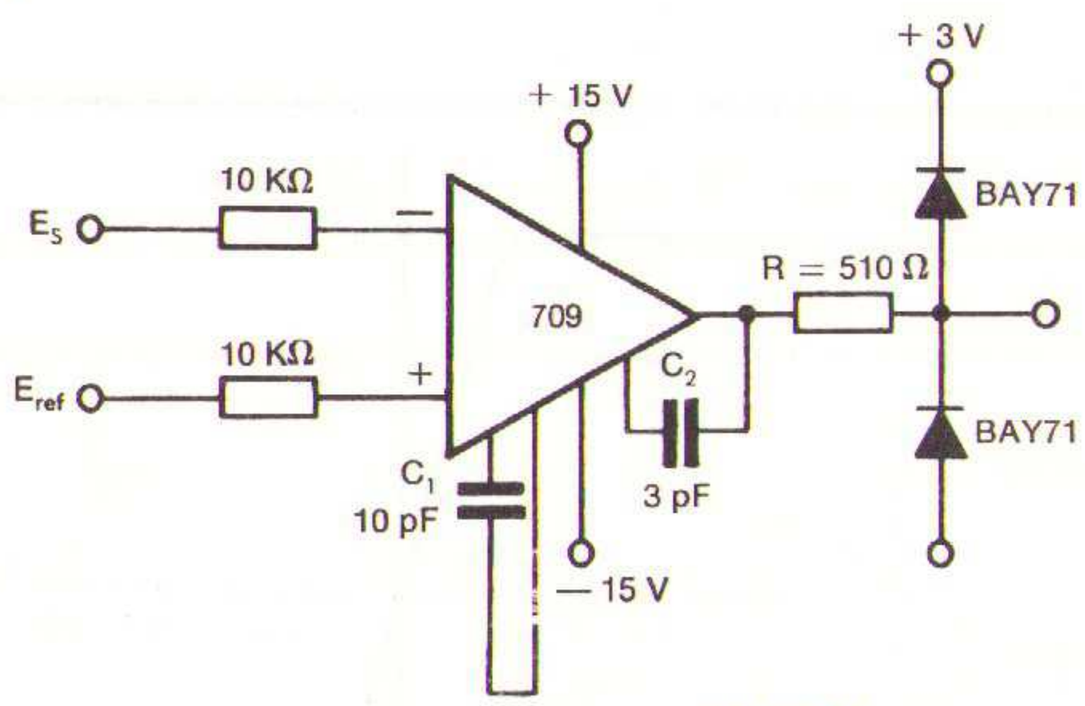


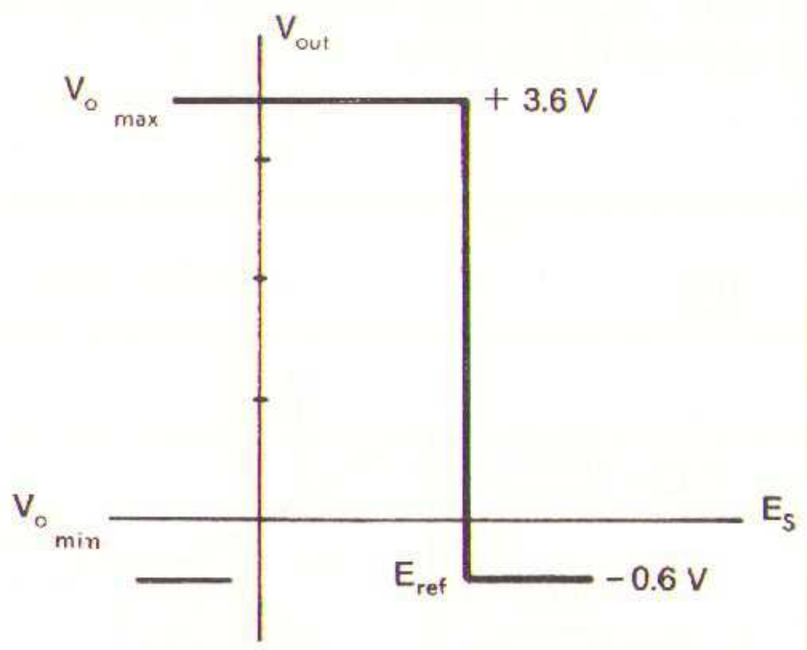
Fig. 3.37 - Response Time for Various Input Overdrives

The comparator response times for output voltages which vary negatively or positively, are shown in Fig. 3.37 (c) and in (d) for different values of overdrive voltages (for response-time definition refer to the μA710 data sheet).

The comparator output can be kept compatible with digital integrated circuits using the circuit shown in Fig. 3.37 (e) and (f) where the resistor R = (510 Ω) limits the μA709 output current.



(e) circuit



(f) transfer function

Fig. 3.37 - Voltage Level Detector

3.4.3 Voltage Comparator with Hysteresis

For applications where a certain amount of noise is superimposed it is desiderable to have a certain hysteresis in the transfer characteristic.

The hysteresis is obtained by means of positive feedback applied between output and input.

These comparators are also useful in all cases where the input signal varies very slowly.

In fact, for the hysteresis comparator, the time to change from one state to the other is independent as a first approximation , of the input signal; for the comparator described in paragraph 3.4.2 the time

necessary to change from one state to the other is strictly dependent on the rate of change of the input voltage.

Fig. 3.38 shows a comparator with a hysteresis cycle using the μA709 arranged in order to have the output compatible with integrated digital circuits.

The hysteresis cycle V_H is given by:

$$V_H = \frac{\Delta V_o}{A_C} \cong \Delta V_o \beta$$

where:

$$\beta = \frac{R_1}{R_1 + R_2}$$

and:

$$\Delta V_o = V_{o\,max} - V_{o\,min}$$

By the use of the μA709 element, comparators which are sufficiently accurate with a hysteresis cycle in the order of a few millivolts can be designed.

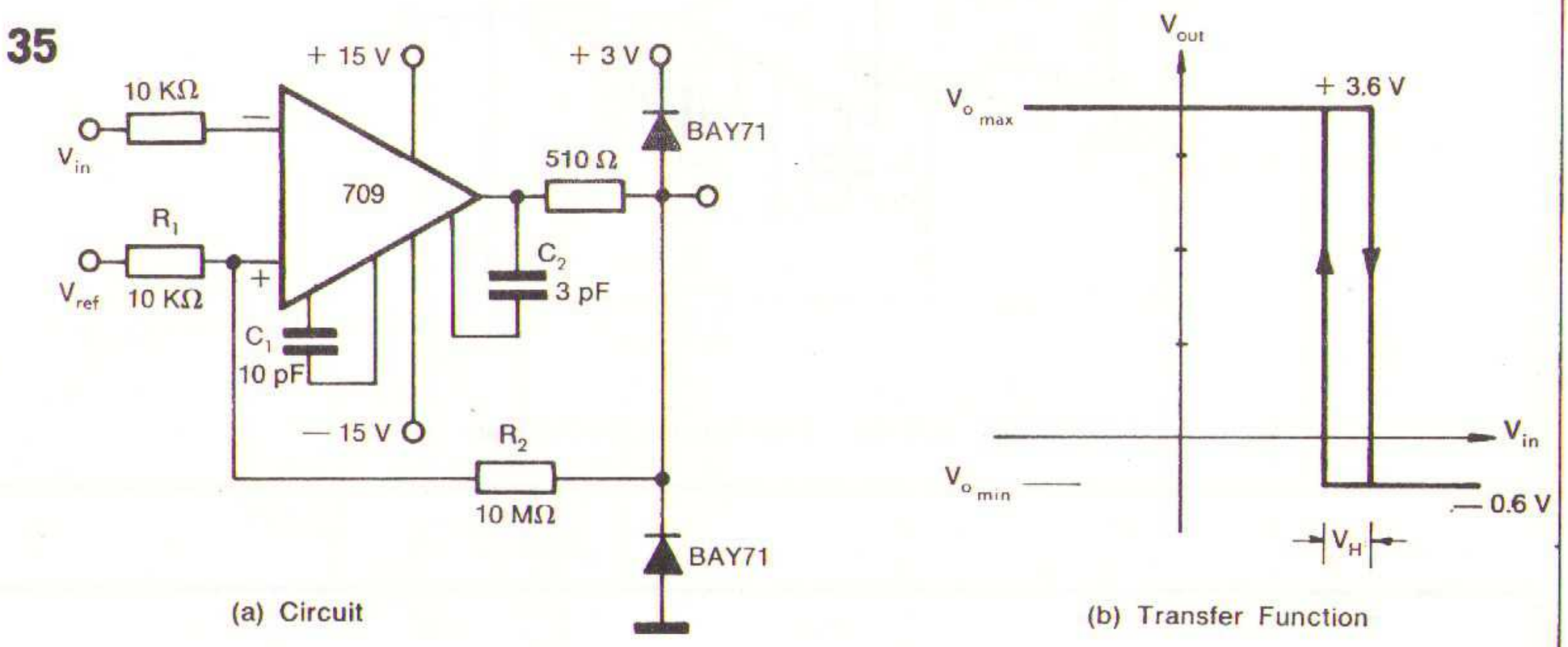


Fig. 3.38 - Level Detector with hysteresis

3.4.4 Astable Multivibrator

Fig. 3.39 (a) shows the circuit diagram of an astable multivibrator using the μA709 integrated amplifier.

The circuit has two states: in one the output is at positive saturation level, in the other at negative saturation level.

Assuming, for instance, that when starting, the μA709 output reaches the positive saturation level, this is due to the effects of positive feedback produced across the voltage divider R_1 and R_2, as the capacitor C across the resistor R is positively charged. When the inverting input voltage reaches the same value as the non-inverting input one, given by:

$$V^+_{o\,max} \frac{R_1}{R_1 + R_2}$$

the circuit switches very quickly to the negative saturation level.

In this new state the non-inverting input is kept at the voltage:

$$V^-_{o\,max} \frac{R_1}{R_1 + R_2}$$

Therefore the inverting input remains at the potential of the capacitor charged to the voltage:

$$V^+_{o\,max} \frac{R_1}{R_1 + R_2}$$

because the switching took place very quickly. The circuit therefore, remains at the negative state for the time necessary to discharge the capacitor and to charge it approximately to:

$$V^-_{o\,max} \frac{R_1}{R_1 + R_2}$$

through the resistor R.

The oscillation period is given by:

$$\tau = RC \log_e \frac{(V^+_{o\,max} - V^-_{o\,max}\beta)}{V^+_{o\,max}(1-\beta)} \cdot \frac{(V^-_{o\,max} - V^+_{o\,max}\beta)}{V^-_{o\,max}(1-\beta)}$$

where $\beta = \frac{R_1}{R_1 + R_2}$

which for a symmetrical output amplifier, is:

$$\tau = 2RC\log_e\left(1 + 2\frac{R_1}{R_2}\right)$$

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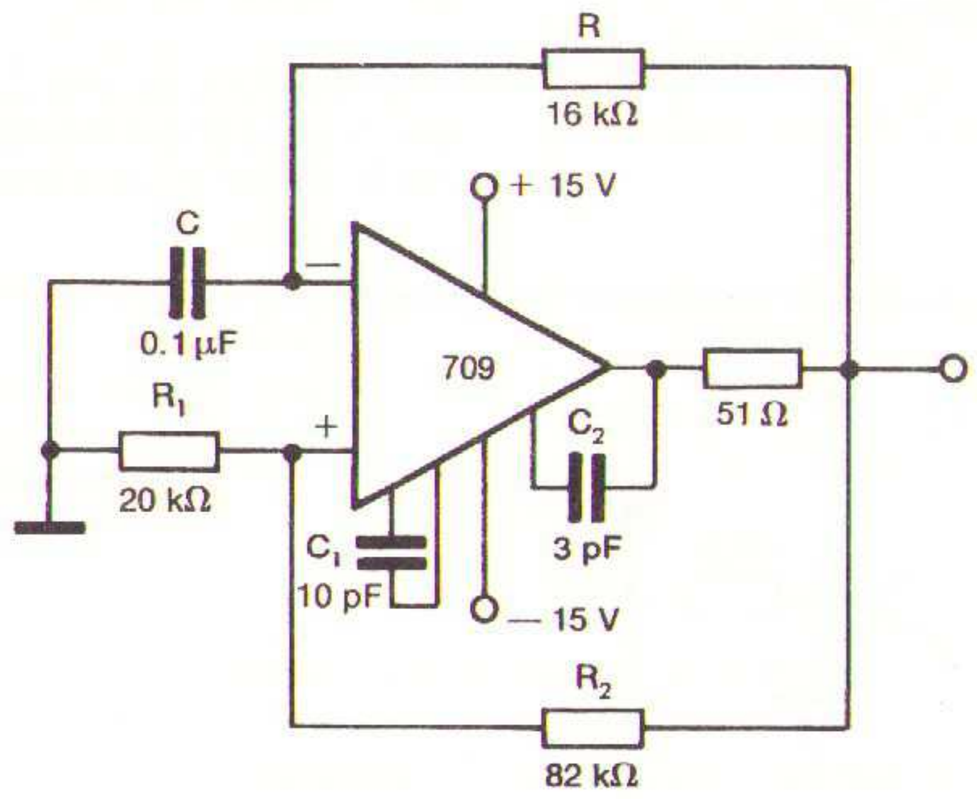

Fig. 3.39 (a) - Free Running Multivibrator

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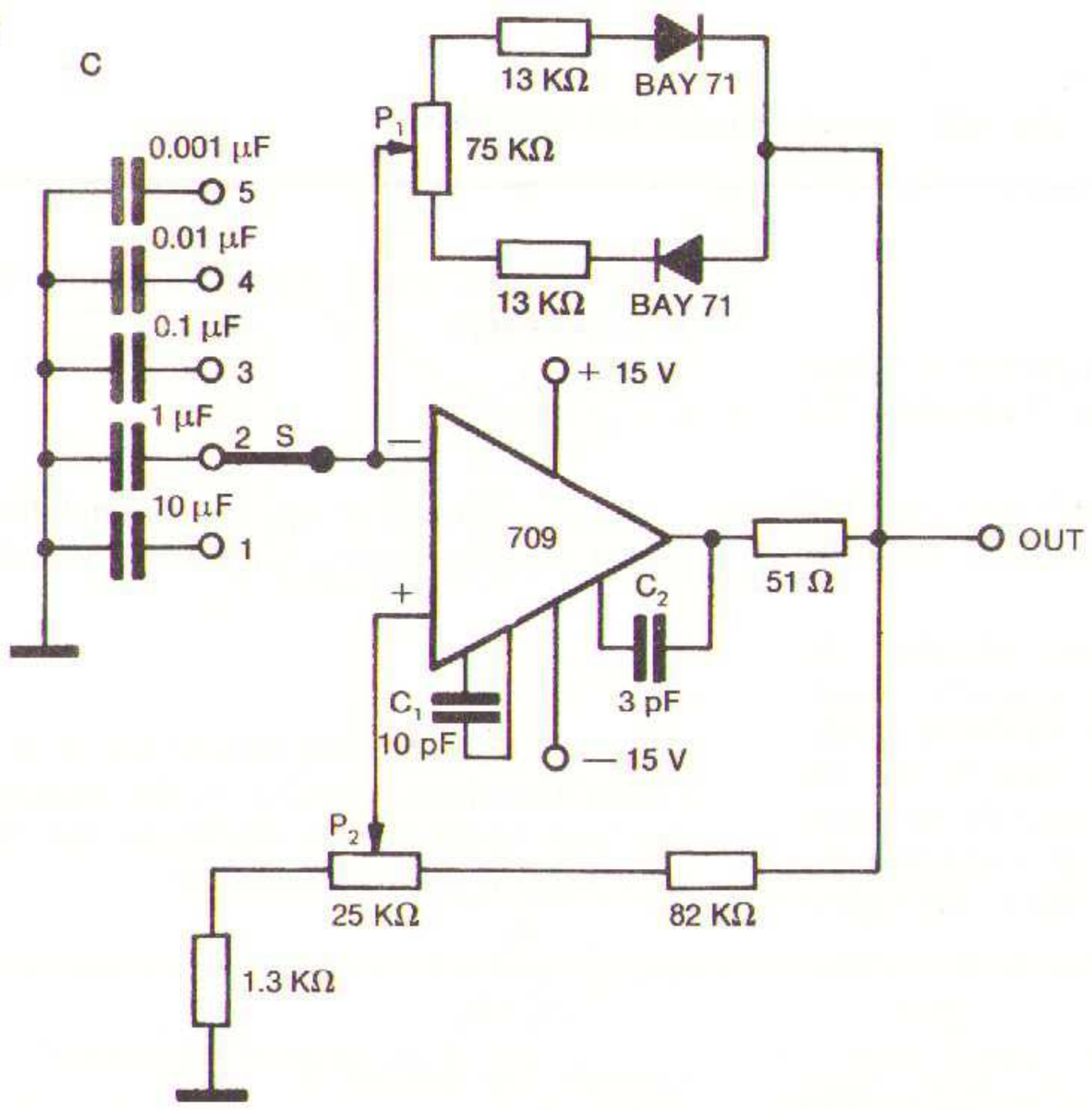


S position	f Hz
1	2-20
2	20-200
3	200-2 K
4	2 K-20 K
5	≥ 20 K

Fig. 3.39 (b) - Square Wave Generator

This multivibrator has excellent frequency stability characteristics (better than 1%₀ for supply voltages variations of a few percent).

Finally, Fig. 3.39 (b) shows a square-wave generator. The fine frequency adjustment is made by potentiometer P_1 which varies the hysteresis cycle, while the coarse adjustment is obtained by switching the capacitors C.

Potentiometer P_2 is used to vary square wave duty-cycle.

It should be noted that the multivibrator stability decreases by some percent by the addition of diodes and potentiometers.

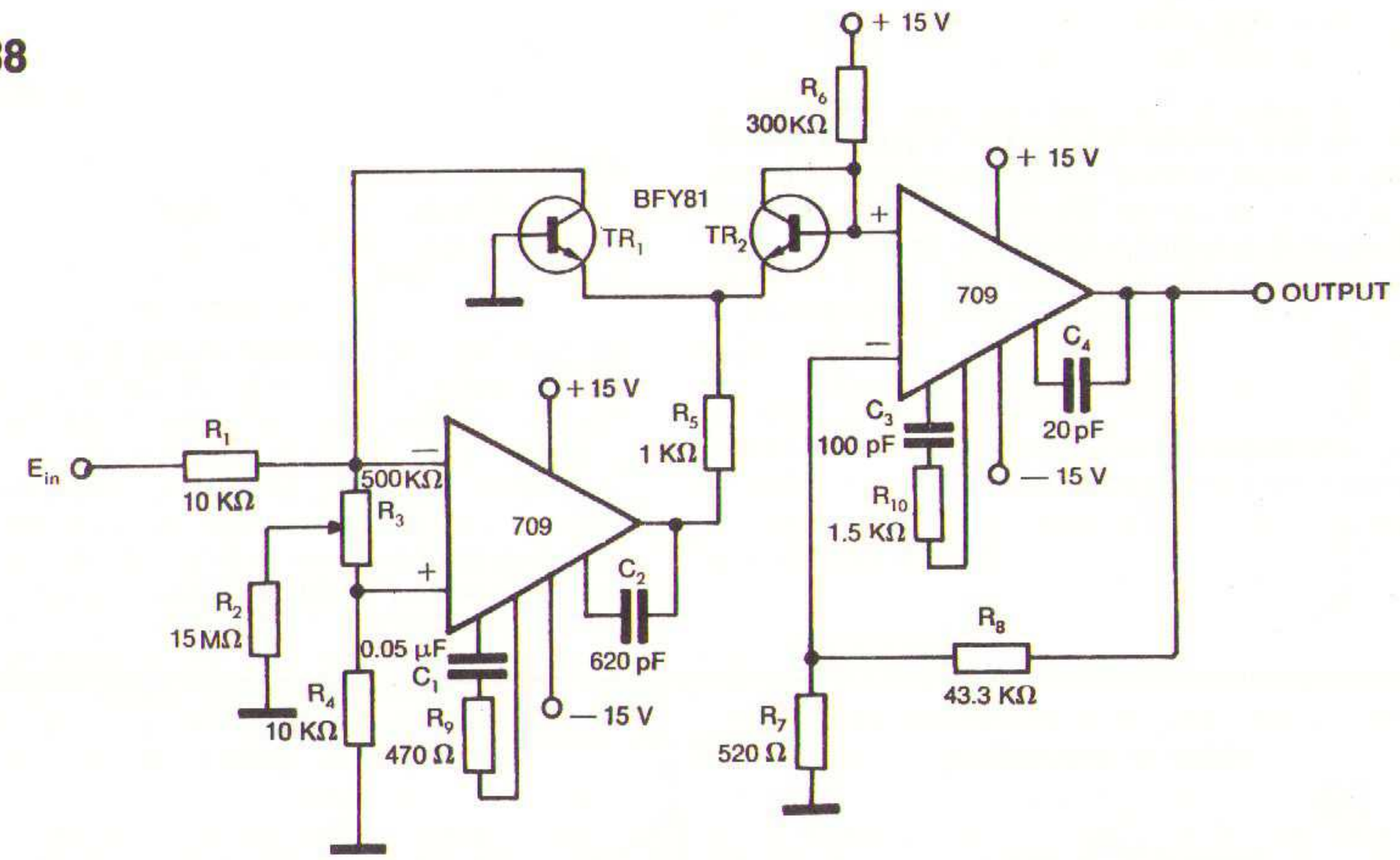


Fig. 3.40 (a) - Logarithmic Amplifier

3.4.5 Logarithmic Amplifier

The bipolar transistor is probably the most predictable non-linear element know to physics. In fact it is known that the variation in collector current with emitter-base voltage is given by

$$I_C \propto \exp\left(\frac{qV_{BE}}{kT}\right) \qquad \ldots\ldots\ldots\ldots (1)$$

where $V_{BE} > \frac{4kT}{q}$

In this equation, q is the charge of an electron, k is Boltzmann's constant and T is the absolute temperature. The expression holds up to high currents where emitter contact and base spreading resistances become important and down to low currents where collector leakages cause inaccuracy. The expression is valid for operation over at least nine

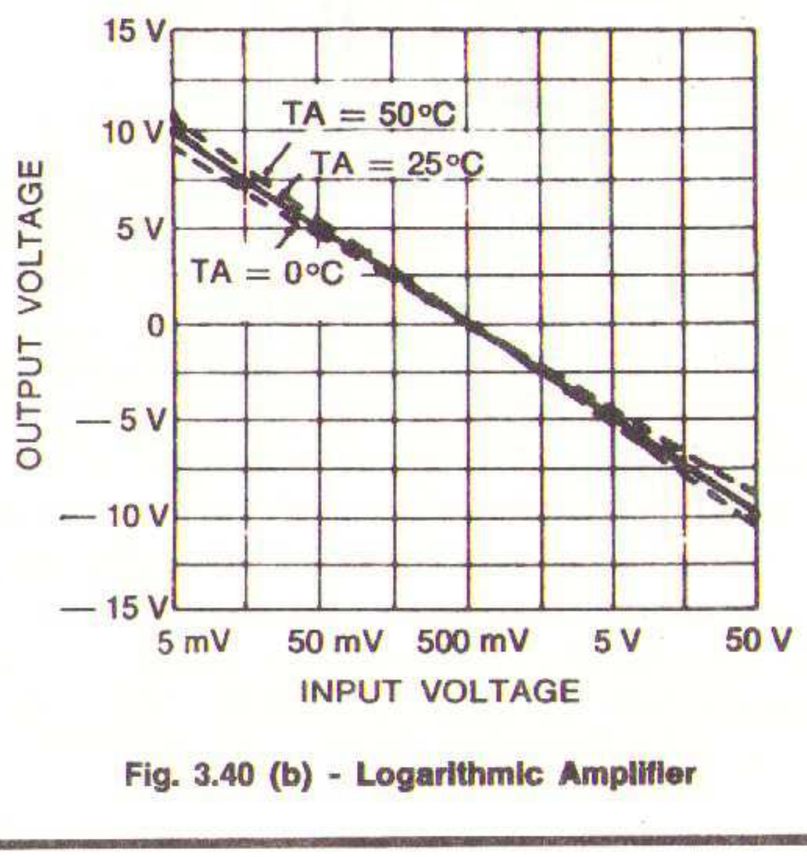


Fig. 3.40 (b) - Logarithmic Amplifier

decades of collector current with well-made silicon transistors. This contrasts with similar expressions for diode current and the emitter current of transistors which show substantial error over three decades of current operation.

Using the expression given above, it can be shown that the emitter-base voltage differential between two matched transistors operating at different collector currents is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \quad \ldots\ldots\ldots (2)$$

In the circuit of Fig. 3.40 (a), a transistor TR_1 is used as the feedback element around a μA709 operational amplifier. The negative feedback forces the collector current of TR_1 to be equal to the current into the summing node of the amplifier. Hence, we can write

$$I_{C1} = \frac{E_{in}}{R_1} \quad \ldots\ldots\ldots\ldots (3)$$

The collector current of TR_2 is determined by the positive supply voltage and R_6 as

$$I_{C2} = \frac{V^+}{R_6} \quad \ldots\ldots\ldots (4)$$

If TR_1 and TR_2 are a matched pair of transistors, Eq. (2) can be used to give

$$\Delta V_{BE} = \frac{kT}{q} \log_e \left(\frac{R_6 E_{in}}{R_1 V^+} \right) \quad \ldots\ldots\ldots (5)$$

Since the base of TR_1 is grounded, the negative of this voltage is presented to the input of the second amplifier. The gain of this stage is

$$A_V = \frac{R_7 + R_8}{R_7}$$

so

$$E_{OUT} = \frac{kT(R_7 + R_8)}{q R_7} \log_e \frac{R_6 E_{in}}{R_1 V^+} \quad \ldots\ldots\ldots (6)$$

which shows that the output voltage is proportional to the logarithm of the input voltage. It can be seen from Eq. (6) that the coefficient of the log term is proportional to absolute temperature, which gives it a thermal sensitivity of 0.3%/°C. The overall transfer function of the amplifier is given for various operating temperatures in Fig. 3.40 (b). As shown, the amplifier has an 80 dB dynamic range.

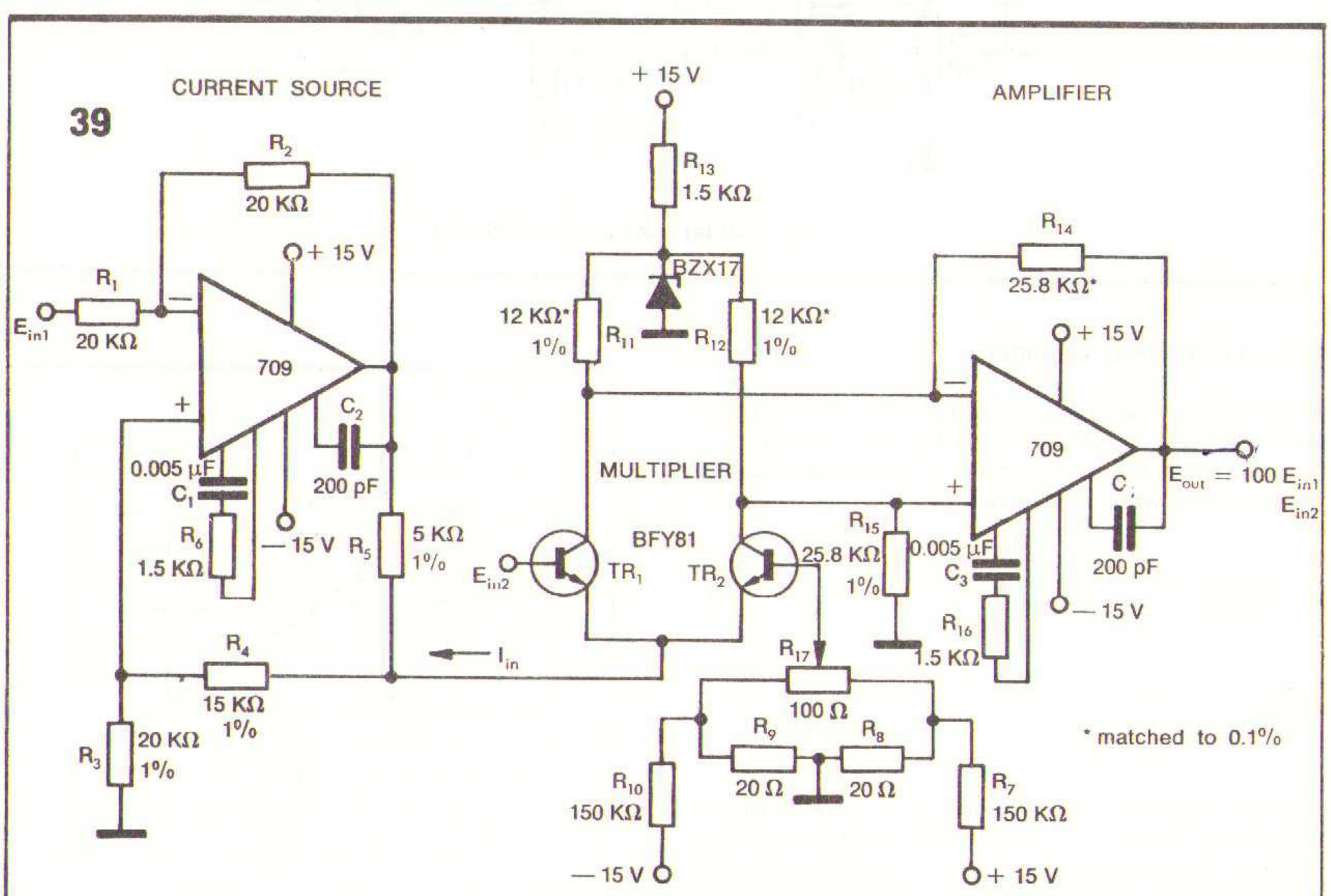


Fig. 3.41 - Multipler

Additional details of the circuit in Fig. 3.40 (a) are that R_2 and R_3 are used to provide an offset adjustment, which increases the dynamic range for small input signals. R_5 is used to limit the loop-gain of the input amplifier so that it can be frequency compensated. R_7 is chosen to be equal to the diode impedance of TR_2 to minimise the effect of the input bias current of the output amplifier. The slope of the log characteristic is determined by R_8 while R_6 determines the zero crossing.

3.4.6 Multiplier

Another interesting use for the non linear properties of the bipolar transistor is the multiplier shown in Fig. 3.41. The basic multiplying element is the transistor pair, TR_1 and TR_2. Its operation can be understood from the following:

The small signal transconductance of a transistor is given by:

$$\frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT} \qquad \ldots\ldots\ldots (1)$$

A matched transistor pair in a differential configuration as shown in Fig. 3.41 will now be considered. For zero differential input voltage, the input current supplied to the emitters will split equally between the two transistors and the differential output current will be zero. Hence, Eq. (1) can be rewritten in terms of the differential output current, the input current to the emitters, and the input voltage as

$$I_{OUT} = \frac{q}{2kT} I_{IN}\ I_{IN2} \qquad \ldots\ldots\ldots (2)$$

Hence, the differential output current is proportional to the product of the differential input voltage and the current supplied to the emitters.

In Fig. 3.41, the first μA709 supplies a current that is proportional to a positive input voltage to the emitters of TR_1 and TR_2. Using standard operational amplifier theory, this current can be shown to be

$$I_{IN} = \frac{E_{IN1}\ R_2}{R_5\ R_1} \qquad \ldots\ldots\ldots (3)$$

A second input voltage is supplied to the differential pair. Combining Eqs. (2) and (3) and setting $R_1 = R_2$ the output current of the differential pair is

$$I_{OUT} = \frac{q}{2kTR_5} E_{IN1}\ E_{IN2} \qquad \ldots\ldots\ldots (4)$$

The output of the pair is connected to a second μA709 that converts the differential current to a single-ended, zero referred voltage.

The output voltage of this amplifier will be $E_{out} = = R_{14}\ I_{out}$, for $R_{14} = R_{15}$ and $R_{11} = R_{12}$. Hence,

$$E_{out} = \frac{qR_{14}}{2kTR_5} E_{IN1}\ E_{IN2} \qquad \ldots\ldots\ldots (5)$$

which shows that the output voltage is proportional to the product of the two input voltages.

There are several hints that are pertinent to making the circuit work right. One is that the resistor pairs R_{11}, R_{12} and R_{14}, R_{15} must be very closely matched (within 0.1 percent). An adjustment is provided for nulling the offset of TR_1 and TR_2. This adjustment should be made when the current-source current is at its maximum value. It should also be noted that Eq. (2) is a small-signal approximation, so the voltage input to the differential pair should be kept small. Restricting the input voltage to ± 20 mV gives linearity that is acceptable for the majority of applications. It should also be pointed out that E_{IN2} can be a bipolar signal while E_{IN1} must be a positive voltage.

3.4.7 Microammeter

Fig. 3.42 shows the circuit diagram of a low voltage-drop microammeter using the μA709.

The minimum scale (1μA) is essentially determined by the errors of the amplifier due to the thermal drift and, to a iesser degree, by the low frequency fluctuation and by the maximum allowable voltage drop at the meter terminals (3 mV).

The current through the indicating instrument is extremely accurate due to the high gain of the μA709, and is given by the following:

$$I_o = I_{IN}\ R \frac{R_1 + R_2}{R_1\ R_L} = I_{IN} \frac{R}{3}$$

A 1 mA f.s.d. meter has been used as an indicating instrument in order to make the unit very sturdy.

Potentiometer P_1 is used for zero adjustment in order to compensate for the amplifier offset.

The meter, of very compact construction, is supplied with two batteries of 9 V and the current consumption is kept within very close limits (3 mA). Diodes D_1 and D_2 protect the amplifier and the different meter ranges are set from 1 μA to 100 mA, by means of the the switched input resistors.

The meter has an accuracy of 1% at ambient temperature, this is mainly determined by the quality of the meter, the tolerances of the resistors and with temperature, and has an accury of 0.2%/°C.

40

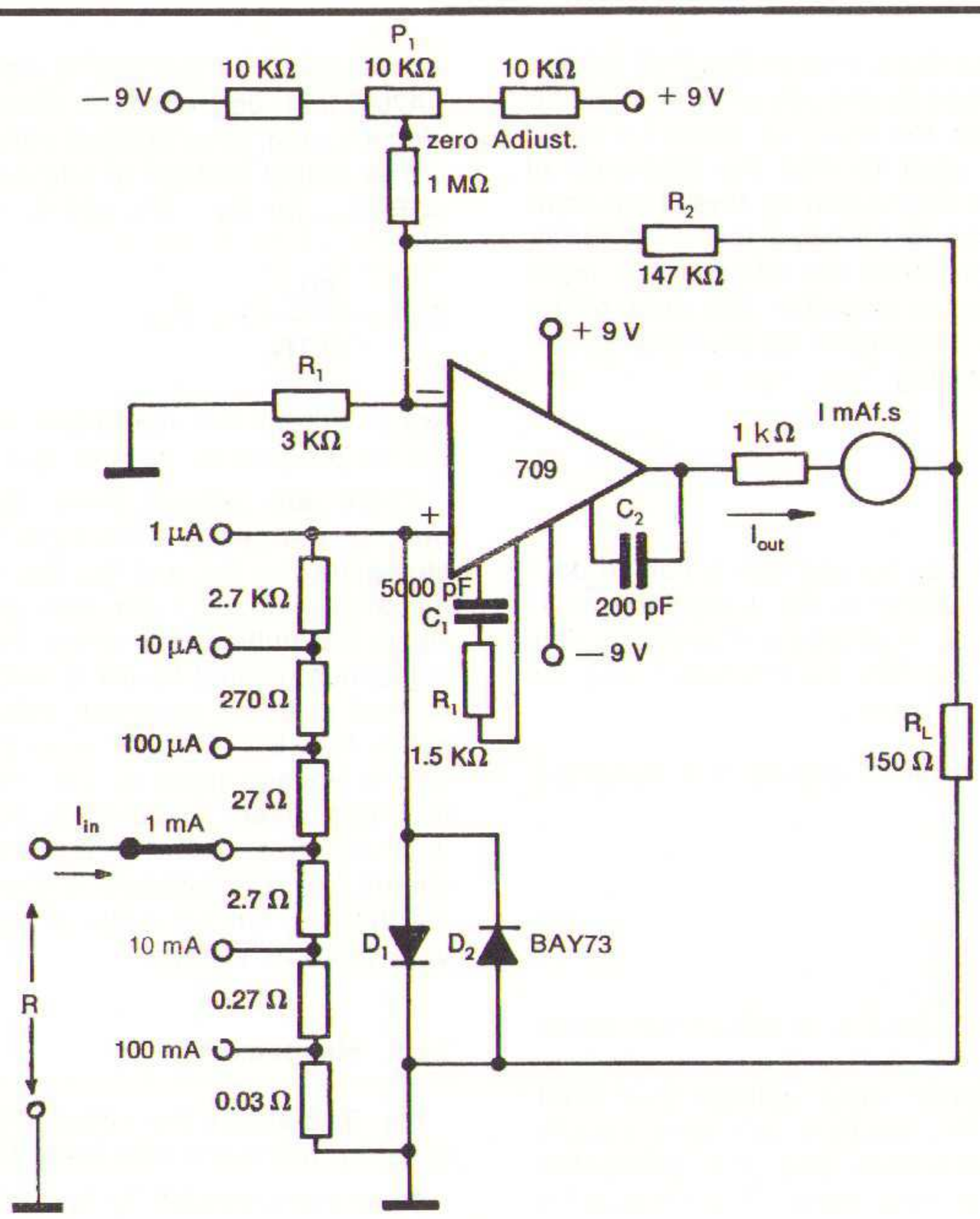
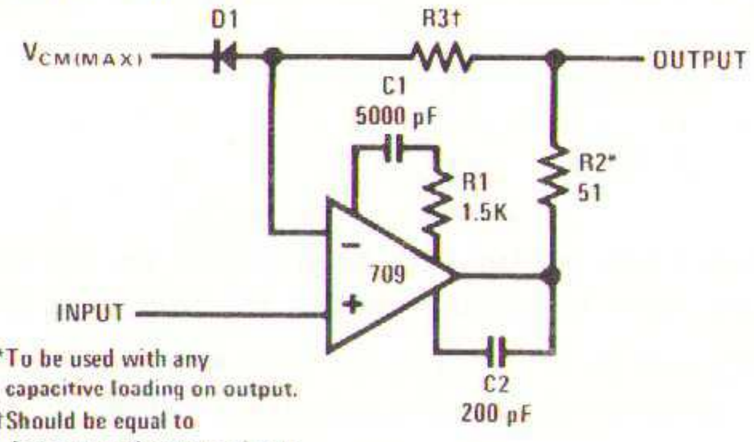


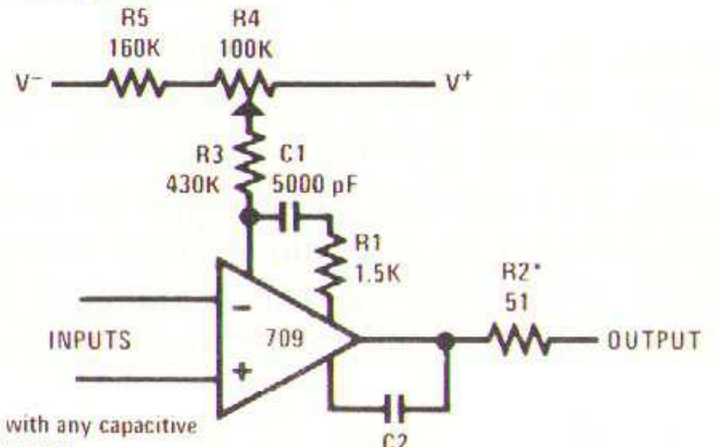
Fig. 3.42 - D.C. Microammeter

41 Voltage Follower



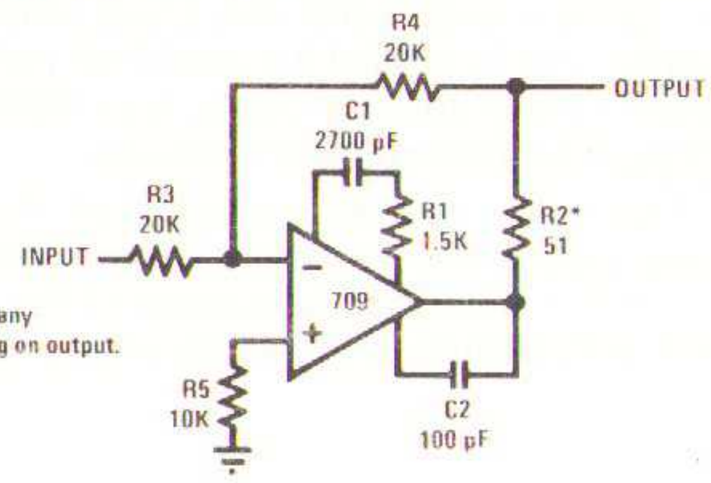
*To be used with any capacitive loading on output.
†Should be equal to dc source resistance on input.

42 Offset Balancing Circuit



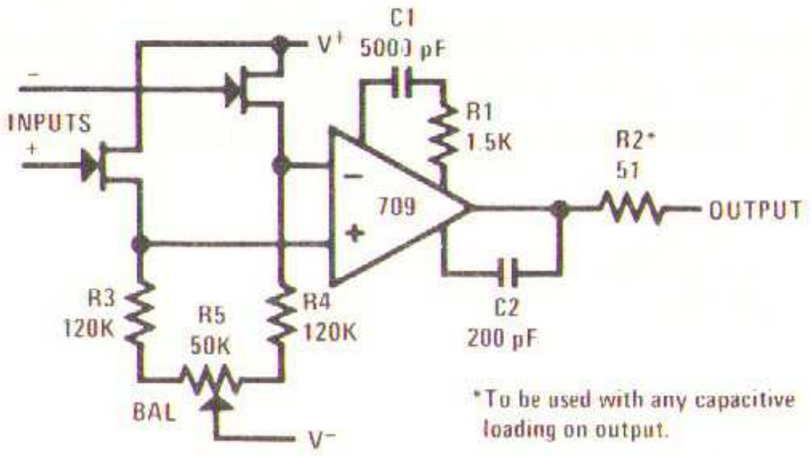
*To be used with any capacitive loading on output.

43 Unity Gain Inverting Amplifier



*To be used with any capacitive loading on output.

44 FET Operational Amplifier



*To be used with any capacitive loading on output.

3.7.6 Double-ended Differential Threshold Detector with Hysteresis

Fig. 3.59 shows a double-ended differential threshold detector. In this circuit hysteresis is provided at both the upper and lower threshold levels. A μA709 operational amplifier serves as both a buffer and a difference amplifier. With component values shown, an output is obtained from the μA711 when the difference between the two input voltages exceed 0.55 V. A hysteresis of approximately 50 mV is obtained.

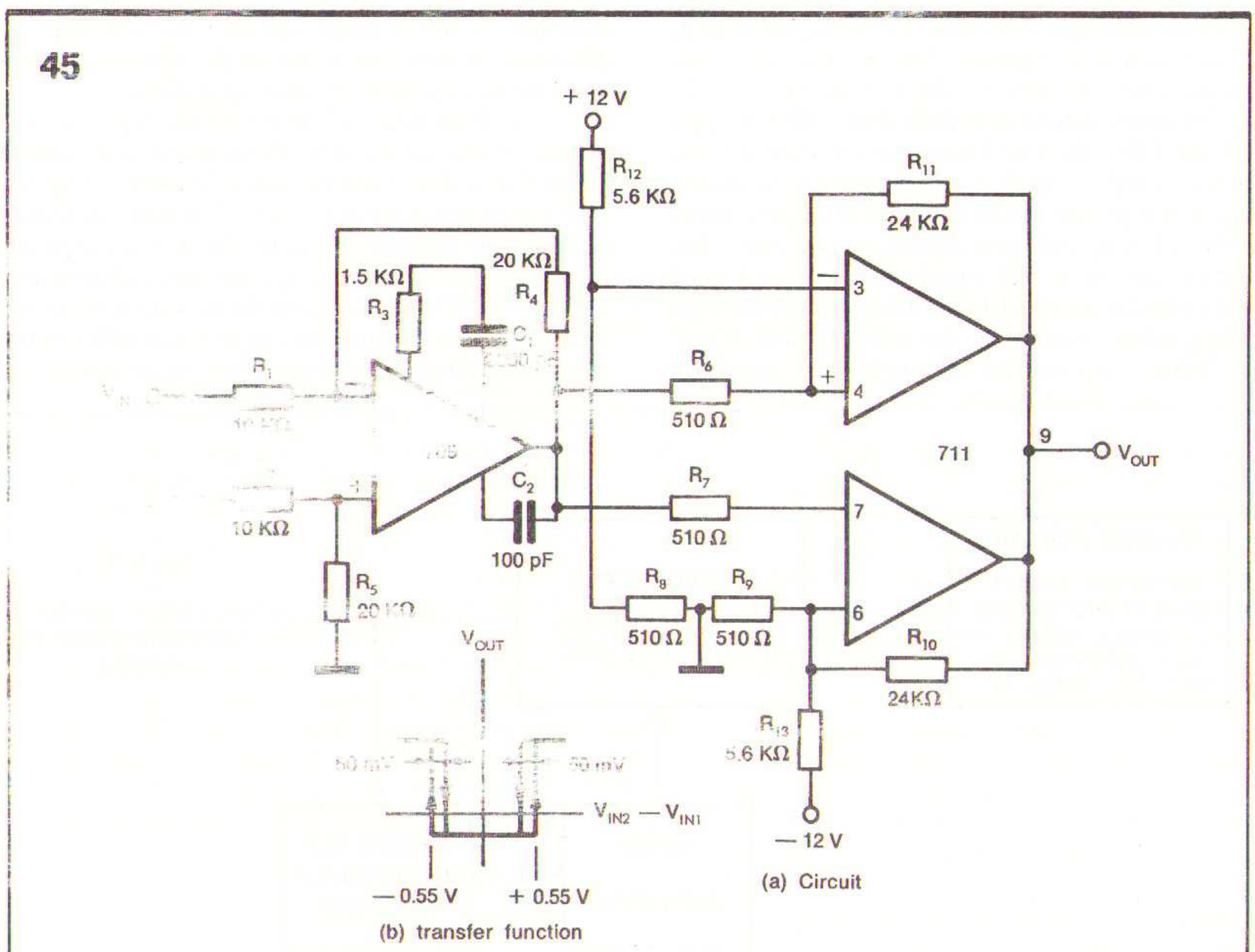


Fig. 3.59 - Double-ended Differential Threshold Detector with Hysteresis

ECONOMICAL POWER VOLTAGE REGULATORS

James M. Garrett

Voltage regulators for power supplies generally use either "series pass" or "switching mode" designs in their output stage. In both designs, selection of the output transistors are an especially crucial factor——trade-offs are required between the cost, power dissipation, and electrical characteristics of the output transistors. In this report, a very useful approach to output stage design is presented that is applicable to a wide variety of voltage regulators. The approach is based on the Texas Instruments series of plastic epitaxial-base single-diffused power transistors. Complete designs are presented and compared for a series-pass and a switching-mode regulator. Both circuits are designed to convert a source voltage to a lower voltage (up to 40 V) regulated against load fluctuations from 0 to 10 A. The switching-mode regulator handles not only load fluctuations but also source voltages from 30 to 50 V.

The output transistors in both designs are PNP types TIP34 and TIP32 from the low-cost plastic single-diffused series mentioned. These devices have the low saturation voltage and high gain required by the series-pass output stage for efficiency and good regulation, respectively. The transistors also have fast switching speeds and good secondary-breakdown characteristics (high permissible I_C at high V_{CE} values) required by the switching-mode output stage. These characteristics in combination with high power-dissipation capability and low cost are the keys to this solution of the series-pass and switching-mode voltage-regulator output problem.

The basic voltage-regulator mechanism used in both designs is shown in Figure 1. The significant difference between the two configurations described below is in the output stage.

SERIES-PASS OUTPUT STAGE

A complete voltage regulator with a series-pass output stage is shown in Figure 2. This type of output stage is attractive because it has relatively few components. When efficiency is not a prime consideration and when the difference between source and output voltages is not too great, the series-pass element is a logical choice.

The disadvantage of the series-pass stage is the heat dissipation encountered there. For example, if an output of 1 V at 5 A is desired and the available source voltage is 15 V, the series element must conduct 5 A with a differential of 14 V from collector to emitter. Since power dissipation of a transistor equals V_{CE} I_C, the series element must dissipate 70 W under these conditions. Thus it is apparent that heatsinking requirements can be severe with this type of regulator. (Heat-sink selection is not discussed here.)

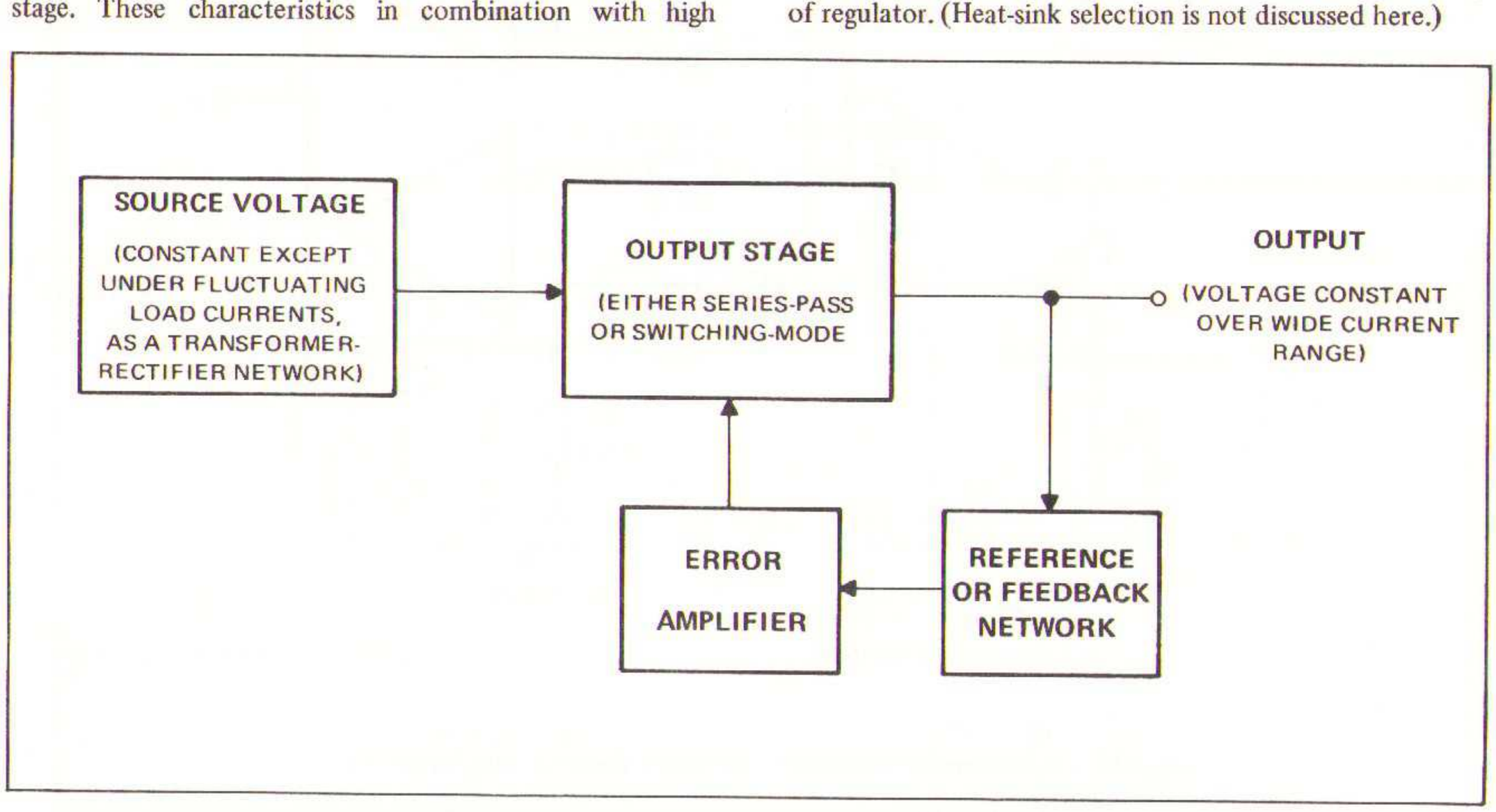


FIGURE 1. Block Diagram of Basic Voltage-Regulator Design

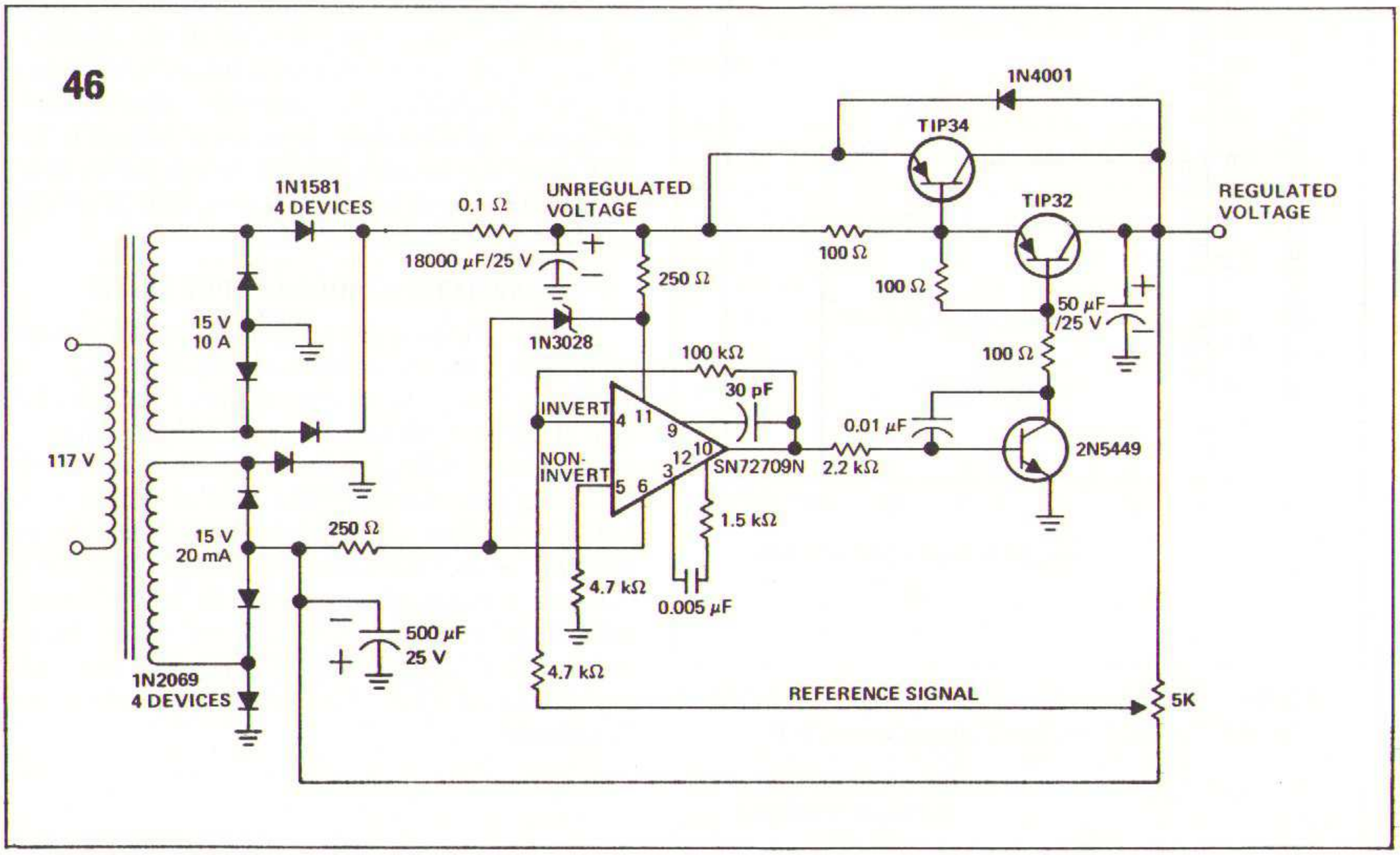


FIGURE 2. A Voltage Regulator with Series-Pass Output Stage Showing Source of Unregulated Voltage

In the design of Figure 2, the output of the power transformer is full-wave-rectified by the diode bridges. The 1N1581 diodes provide a 15-V d-c unregulated input with 10-A capability. The 1N2069 bridge provides the negative voltage necessary to operate the SN72709N linear integrated-circuit amplifier. The reference is obtained from the voltage developed across the 5-K Ω potentiometer at the output. The output voltage is set at some desired level by adjusting the potentiometer. If, for some reason, the output voltage begins to rise above the set value, a fraction ΔV of the increase is passed to the inverting input of the SN72709N. Here the signal is amplified by some factor A and inverted to produce a voltage $-A\Delta V$ at the output of the SN72709. This drop causes the 2N5449 transistor to conduct less heavily by an amount ΔI_C, as follows:

$$\Delta I_C = -A\,\Delta V\,h_{FE}\,\frac{r_{BE} + h_{ie}}{r_{BE}h_{ie}}$$

Where ΔI_C = change in 2N5449 collector current, ΔV = change in voltage at inverting input of SN72709N, h_{FE} = static forward current transfer ratio of 2N5449, r_{BE} = base-emitter resistance of 2N5449 and h_{ie} = small-signal common-emitter input impedance of 2N5449 = $\Delta V_{BE}/\Delta I_B$.

This ΔI_C causes the TIP32 to begin turning off, thus forcing the Darlington-connected TIP34 output device to drop the output voltage toward the original set value.

A capacitor is connected from the collector of the 2N5449 to its base to prevent oscillations. (The single-diffused TIP32 and TIP34 devices have a transition frequency f_T of 3 MHz, so this capacitor compensation is sometimes necessary in low-frequency circuits.)

The graph in Figure 3 shows the power capabilities of the TIP34 device used in this circuit. Currents as large as 10 A can be handled by the output device if the voltage from collector to emitter is held below 8 V according to the safe operating region shown in this figure. Likewise, output voltages up to 40 V can be obtained if the current is held within the indicated limits.

This power supply was designed for low-voltage use. The voltage output can be increased if care is taken to keep the output device within the safe operating region. As the output voltage level is increased, the 100-Ω resistor from the base of the TIP32 to the collector of the 2N5449 should be increased in value to prevent overheating or overdriving the base of the TIP32.

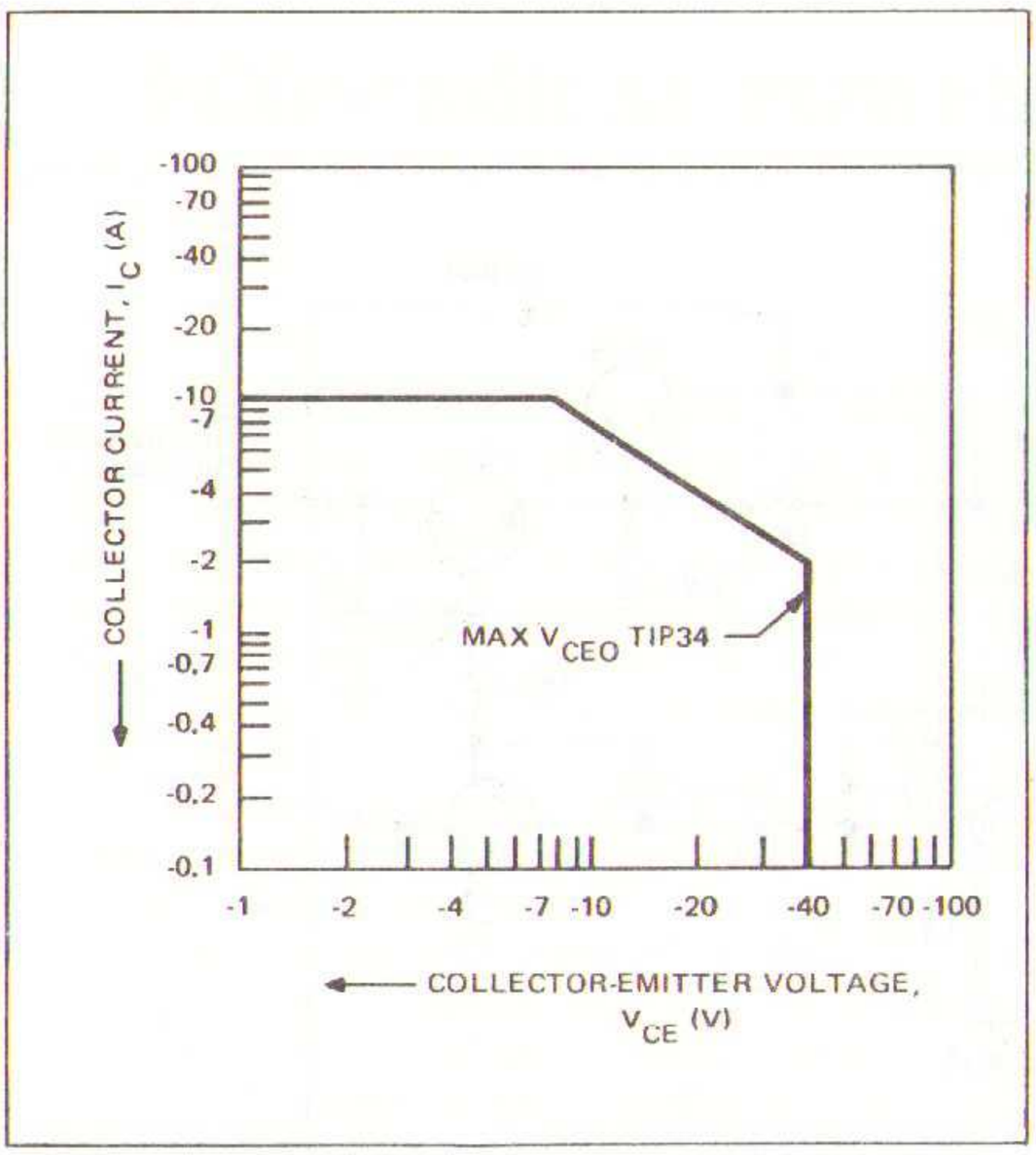


FIGURE 3. Maximum Safe Operating Region of TIP34 in D-C Operation at Case Temperature ⩽ 25°C

The 1N4001 diode is included to protect the TIP 34 output device against damage from reverse voltage surges.

The linear amplifier is the main control element of the system. A feedback network consisting of a 100-K Ω and a 4.7-K Ω resistor sets the gain of the amplifier. An increase of gain may result in oscillations, while a decrease of gain produces less regulation. Measurement of performance of this voltage regulator at outputs from 1 to 10 V shows the output regulation to stay within 10 mV of the setpoint in most cases (never more than 20 mV), under load fluctuations from 0 to 10 A.

SWITCHING-MODE OUTPUT STAGE

When efficiency and low power dissipation are prime requirements, the switching-mode regulator may provide the best solution. An example is shown in Figure 4. This type of circuit regulates the output voltage by pulsing the output current through a smoothing filter by means of a "switching pass element." The ratio of output to input voltage is proportional to the fraction of time the output transistor is *on*. The efficiency is high since the series transistor is practically always in one of two states: *off*, where little dissipation occurs, or *on*, where dissipation amounts to $V_{CE(sat)}I_C$ (Since $V_{CE(sat)}$ of epitaxial-base single-diffused devices is low, little dissipation occurs during *on* intervals).

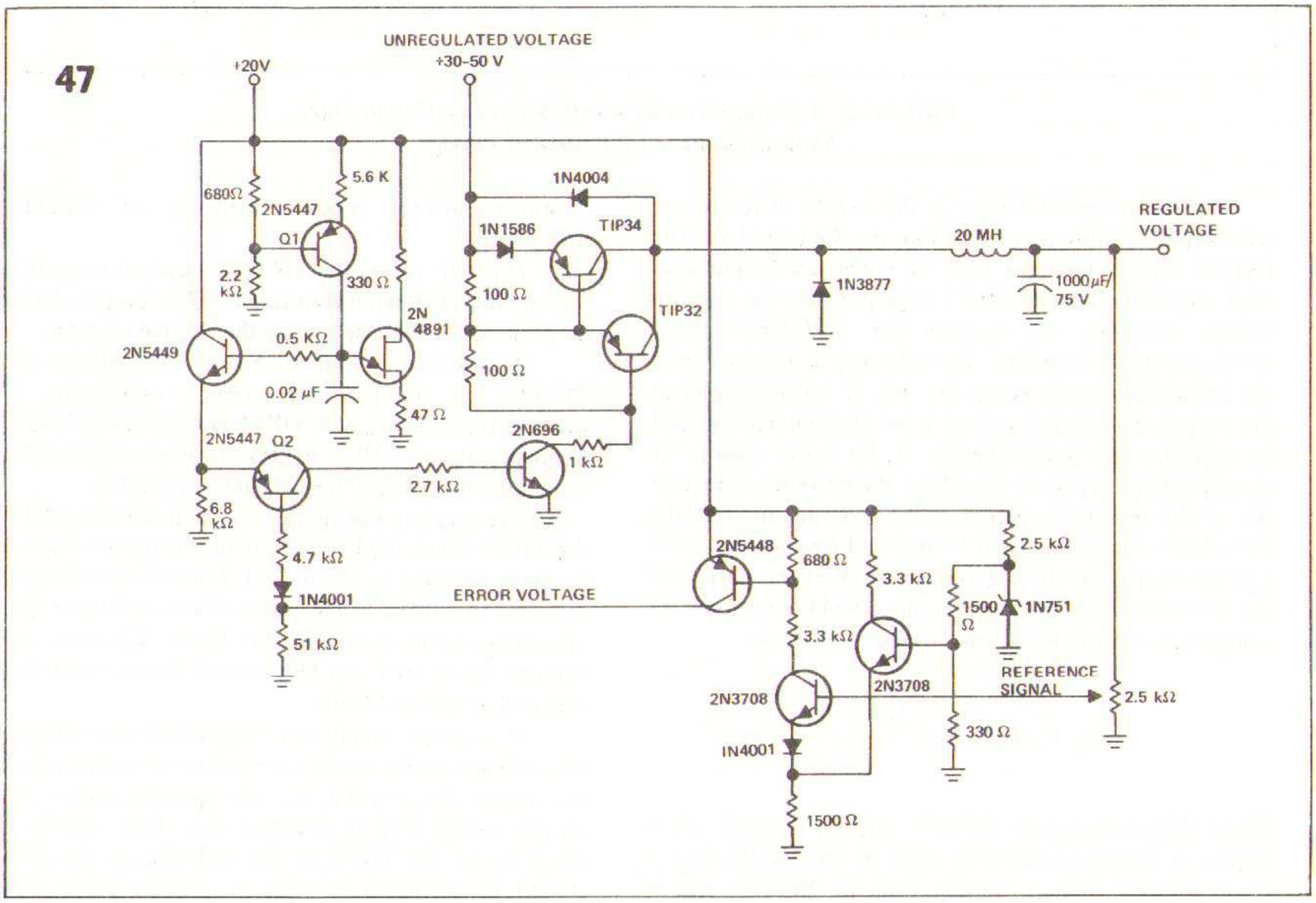


FIGURE 4. A Voltage Regulator with Switching-Mode Output Stage (Not Including Source of Unregulated Voltage)

During the switching interval between *on* and *off*, dissipation in the output device is small because switching times of the output devices are short——on the order of 300 ns. (This epitaxial-base single-diffused transistor series offers the design engineer a significant advantage in minimizing this switching dissipation.) Another factor aiding the efficiency of the switching regulator is energy storage in the inductor. This element transfers its stored energy into the filter capacitor during the interval that the transistor is switched off, resulting in increased efficiency.

Because of a low proportion of power dissipation, this type of supply may require only a small amount of heatsinking. Furthermore, relatively little filtering is required at the switching rates of 2 to 10 kHz encountered. Generally, a switching-mode power supply can provide greater output current with a greater voltage differential between input and output than a series-pass design using the same type of output transistor. Sometimes these advantages are offset by the disadvantages of the circuit, such as increased complexity caused by the requirement of a switching driver and the need for an inductor which is sometimes large and expensive.

In the design of Figure 4, the 2N4891 unijunction transistor is designed to provide a frequency of oscillation around 2 kHz. The 2N5447 (Q1) is used as a constant current source to charge the capacitor on the emitter of the 2N4891. This arrangement provides a linear sawtooth voltage waveform at the emitter, with a peak voltage of approximately $\eta\ V_{BB} = 16$ V. This sawtooth (as shown in Figure 5) is amplified by the 2N5449 connected as an emitter follower. The output across the 6.8-K Ω resistor is used as a current supply for a 2N5447 (Q2). This transistor is wired so that it passes current when its emitter voltage rises to within approximately 0.7 V of its base voltage, which is determined by the error amplifier. When this 2N5447 conducts, it provides base drive which turns on the series element and begins charging the inductor-capacitor combination on the output. On turn-off, the energy stored in the inductor is transferred via the 1N3877 diode into the capacitor.

As the error voltage at the base of the 2N5447 (Q2) is raised or lowered, this transistor begins to conduct earlier or later. Thus the output pulse width and the resultant output voltage are varied. This mechanism is illustrated in Figure 5. (When the output pulse gets extremely short, its current level rises somewhat, but this behavior has negligible effect on the output voltage.)

The heat dissipation of the output transistor in steady operation can be approximated by adding contributions of the three sequential states as follows:

$$\text{Output device dissipation} = \frac{T_{off}}{T} V_{CE(off)} I_{C(off)} + \frac{T_{on}}{T} V_{CE(sat)} I_C + \frac{T_{sw}}{T} V_{CE(off)} I_C$$

where T_{off} = Time interval the output device is *off*, T = Total time, $V_{CE(off)} = V_{CE}$ of output device during *off* time, $I_{C(off)}$ = collector leakage or I_{CBO}, T_{on} = Time interval the output device is *on*, $V_{CE(sat)} = V_{CE(sat)}$ of output device during *on* time, I_C = collector current in output device during *on* time, and T_{sw} = Time occupied in switching.

From this equation it can be seen that switching times and $V_{CE(sat)}$ are probably the largest contributors to device dissipation.

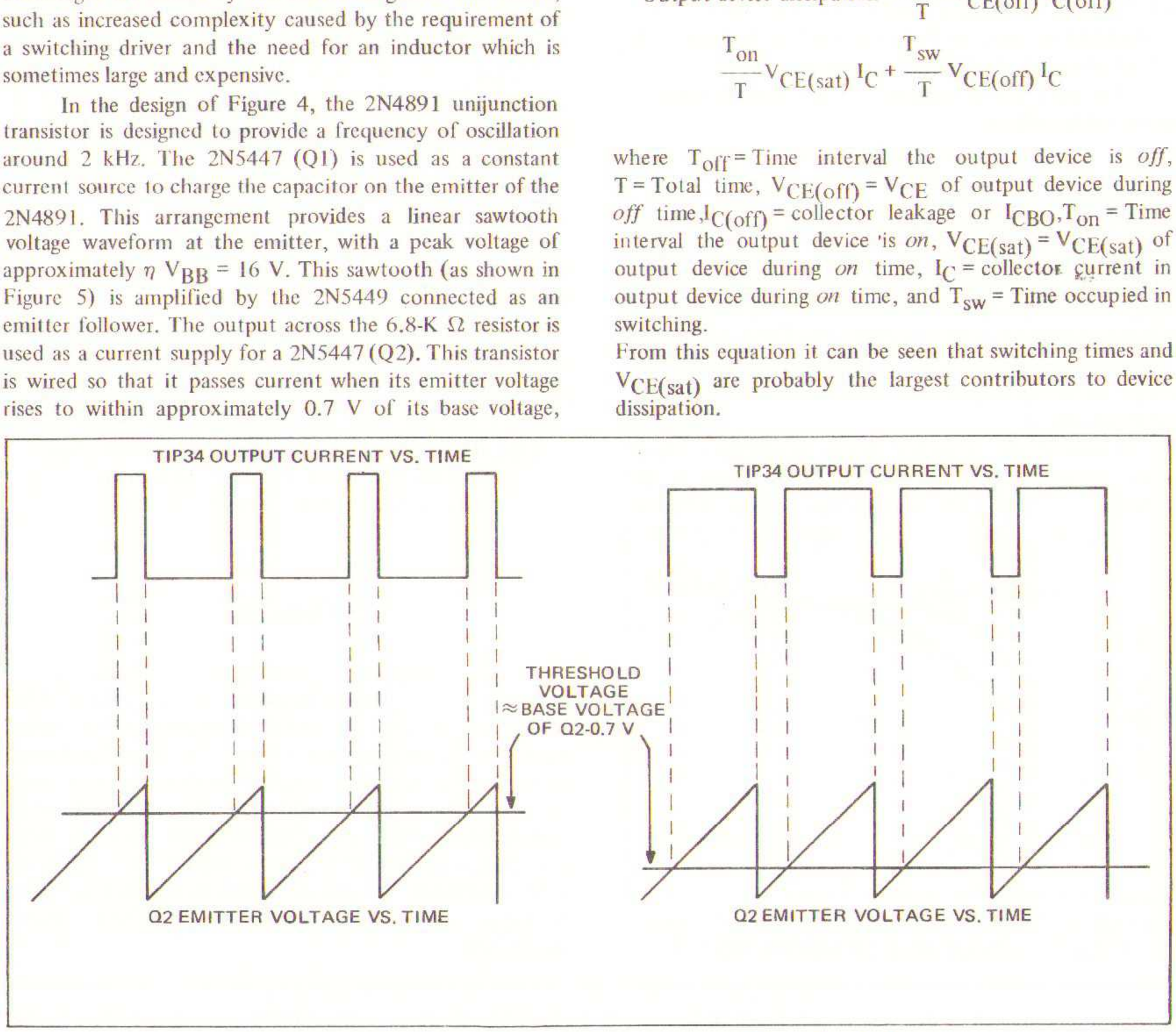


FIGURE 5. Dependence of Output Transistor Pulse Width on Base Voltage of Q2 in Switching-Mode Regulator of Figure 4

The inductor used in the output line can cause some problems if not designed properly. If it is too small, for example, it will saturate and the current developed in charging the filter capacitor may be sufficient to destroy the output device.

Inductive components in switching-mode regulators can cause other problems associated with the secondary-breakdown characteristics (one factor that might be expected to limit the safe operating region, Figure 3) of the output transistor. It is typical for the data-sheet d-c rating of power transistors to show a safe operating region rating that derates below the d-c power-dissipation rating for higher values of V_{CE}. It should be noted here that the safe operating region rating (Figure 3) for the TIP34 single-diffused transistor used in the present design shows no derating below its d-c power dissipation rating at any point within the V_{CE} range of the device. This characteristic can offer significant advantages for switching-mode application.

The output line inductance L (in henries) may be calculated as follows:

$$L = T_{on} (V_{in} - V_{out}) / I_C$$

where T_{on} = time output device is *on*, V_{in} = input supply voltage, V_{out} = output voltage, and I_C = collector current in output transistor during *on* time. The 1N3877 diode connected across the inductor is a fast-switching device which transfers stored energy to the capacitor. The overall regulator efficiency is affected by all of the components in the series path to the output, so this diode reduces circuit efficiency somewhat.

It can be seen from the curves of efficiency versus output voltage (Figure 6) that efficiency drops as the difference between input and output voltage increases.

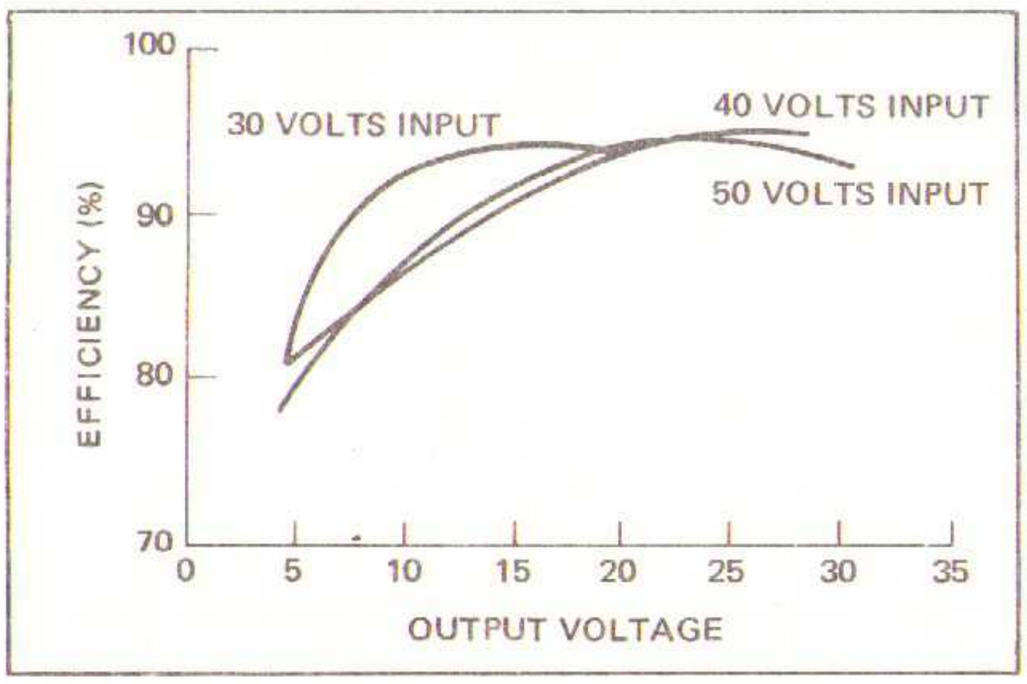


FIGURE 6. Variation of Overall Efficiency with Output Voltage of Switching-Mode Regulator in Figure 4

Efficiency improves as the oscillator frequency is lowered. However, there is a trade-off against excessive values of the inductance and capacitance required on the output at low frequencies.

Figure 6 shows the overall efficiency versus output voltage at various input voltage levels. In this particular design, differentials between input and output voltages on the order of 15 to 30 V can produce efficiencies of 80% to 90%. The drop in efficiency at output voltages below 5 V is because the necessarily short pulse widths result in a small increase in peak current——and since $V_{CE(sat)}$ rises with higher current, the dissipation goes up too.

The regulation precision of this supply is shown in Figure 7. The magnitude of the fluctuations depends mainly on the error-amplifier design. The amplifier shown uses discrete transistors rather than an IC to reduce cost at a minimum sacrifice in precision. Tighter regulation control may be achieved by substituting a higher-gain amplifier.

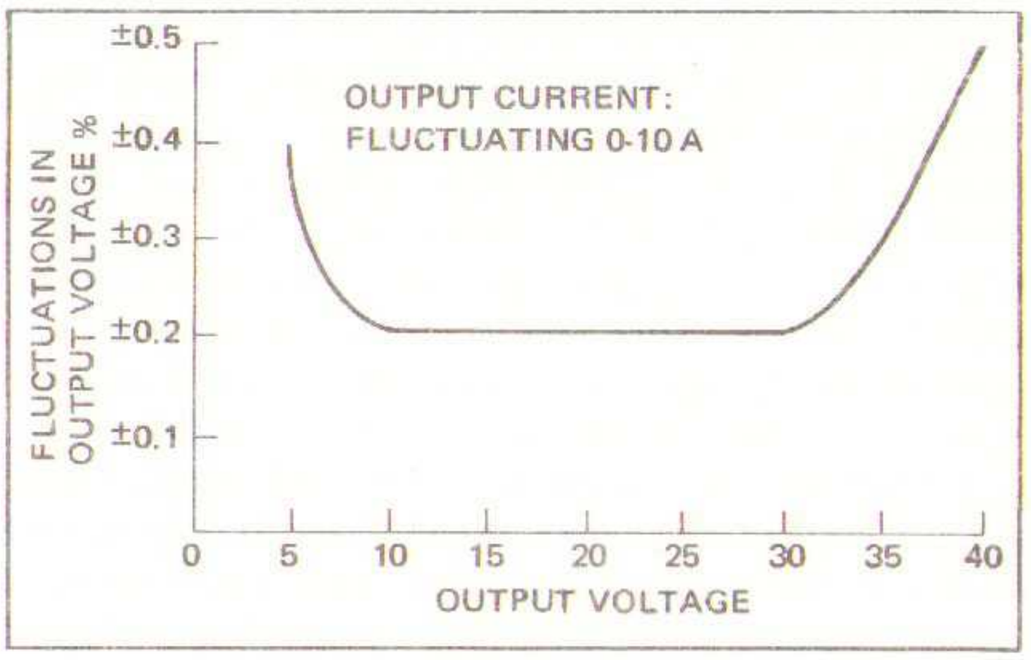


FIGURE 7. Voltage Fluctuations of Switching Mode Regulator (Figure 4) Due to Load Current Fluctuations at Various Output Voltages

SUMMARY

The series-pass regulator offers simplicity in circuitry but has high power-dissipation requirements. The switching-mode regulator design is efficient but requires more control circuitry and filtering. The TI epitaxial-base single-diffused transistor series provides saturation and switching characteristics necessary for either regulator configuration. These advantages combine with low cost, high dissipation capability, and complementary (NPN or PNP) availability to provide excellent performance and flexibility to meet a variety of regulator design requirements.

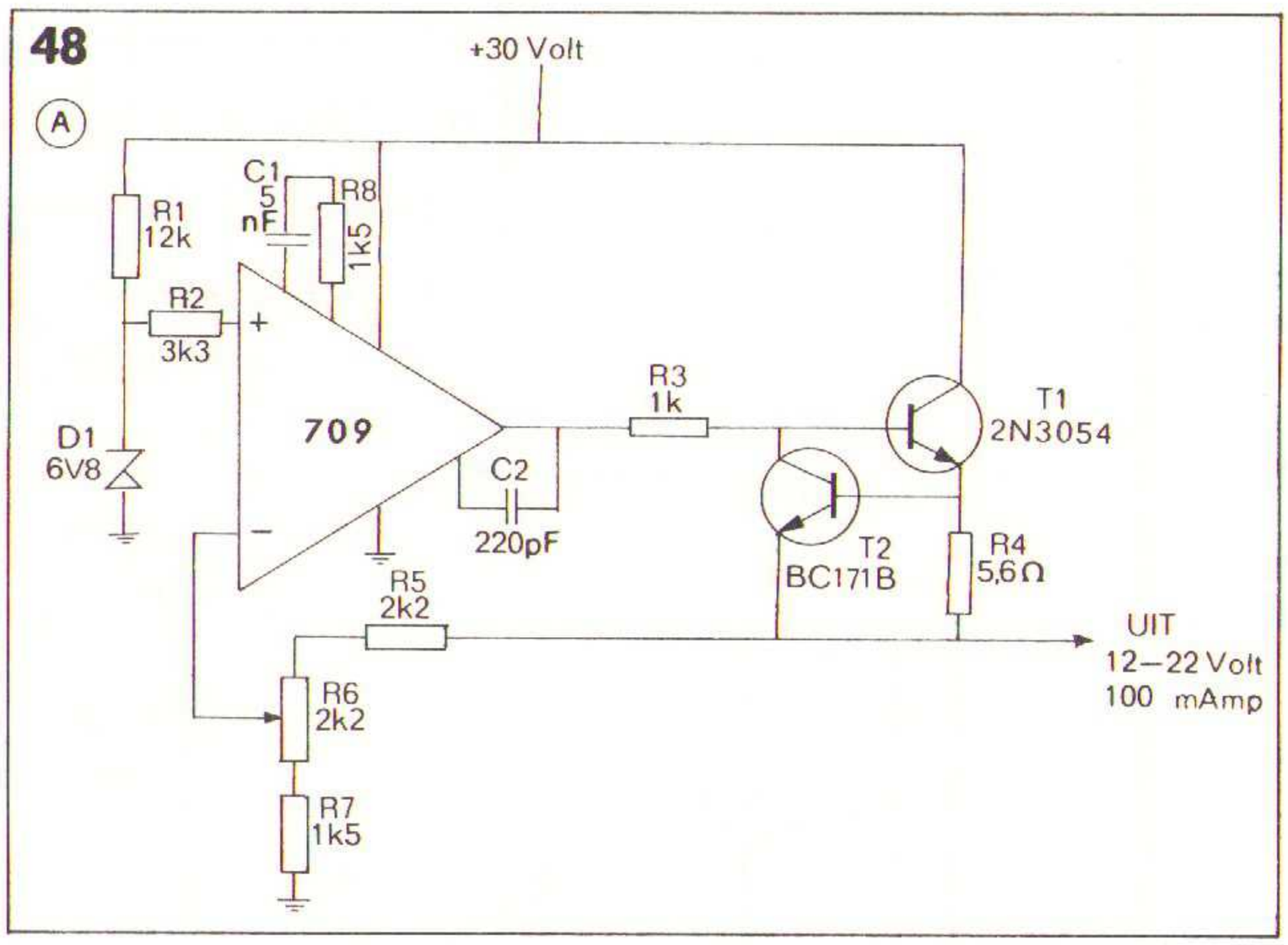
ECONOMICAL POWER VOLTAGE REGULATORS

Although temperature-compensated voltage reference diodes can provide excellent temperature stability, they are only available in rather odd voltage ranges and may have a large tolerance on the actual zener voltage. In addition, the current that can be drawn from these sources without upsetting the temperature coefficient is usually limited to less than 10% of the bias current.

Operational amplifiers can be used as buffers for these references to prevent loading and to provide a convenient means of voltage adjustment. Two possible circuits are shown in Fig. A and B. The circuit of Figure A gives an output voltage greater than the zener reference, and that of Figure B gives an output less than the reference. The high input inpedance, low offset voltage, and low thermal drift of the 709 make possible excellent isolation without degrading the stability of the reference. An interesting feature of the 709 in this application is that it can be operated from a single power supply, and so no negative voltage source is necessary.

An additional emitter-follower, T1, is used at the output to deliver a larger output current than could be supplied by the 709 alone. Output protection is provided by T2, which limits the base drive to T1, when the output current exceeds 100mA. The current limit can be adjusted by varying R4. Figure C shows the output voltage versus output current characteristic of the circuit, and illustrates the excellent regulation obtained up to the current-limiting point. For applications requiring only moderate output capability (10mA), the 709 can be used alone and T1, T2, R3 and R4 can be eliminated from the circuit.

The circuit of Figure B is similar to that just discribed, except the amplifier is operated at unity-gain with its input taken from a tap across the reference diode. Minimum output voltage is limited to 2V to keep the amplifier inputs within their operating common-mode range. Diode D2 protects the amplifier inputs, and C1, C2 and R8 provide frequency compensation (for both circuits).



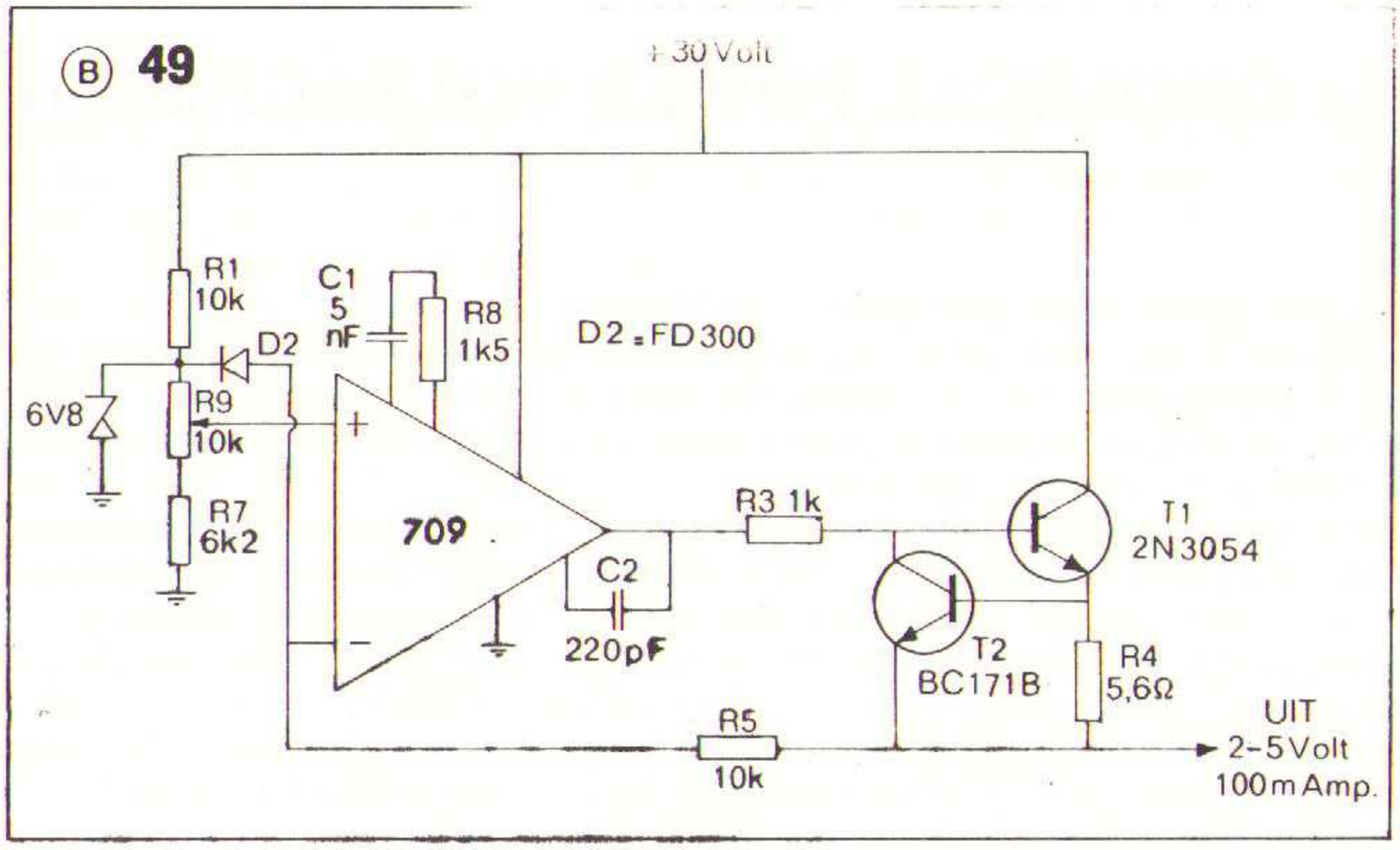
HIGH VOLTAGE SUPPLY.

Normally the 709 is capable of 28Vpp output swings when biased with ±15V supplies. The 100V D.C. regulator circuit shown in figure D usus a single 709 as the control element, but in a modified bootstrap configuration that accomplishes two objectives:

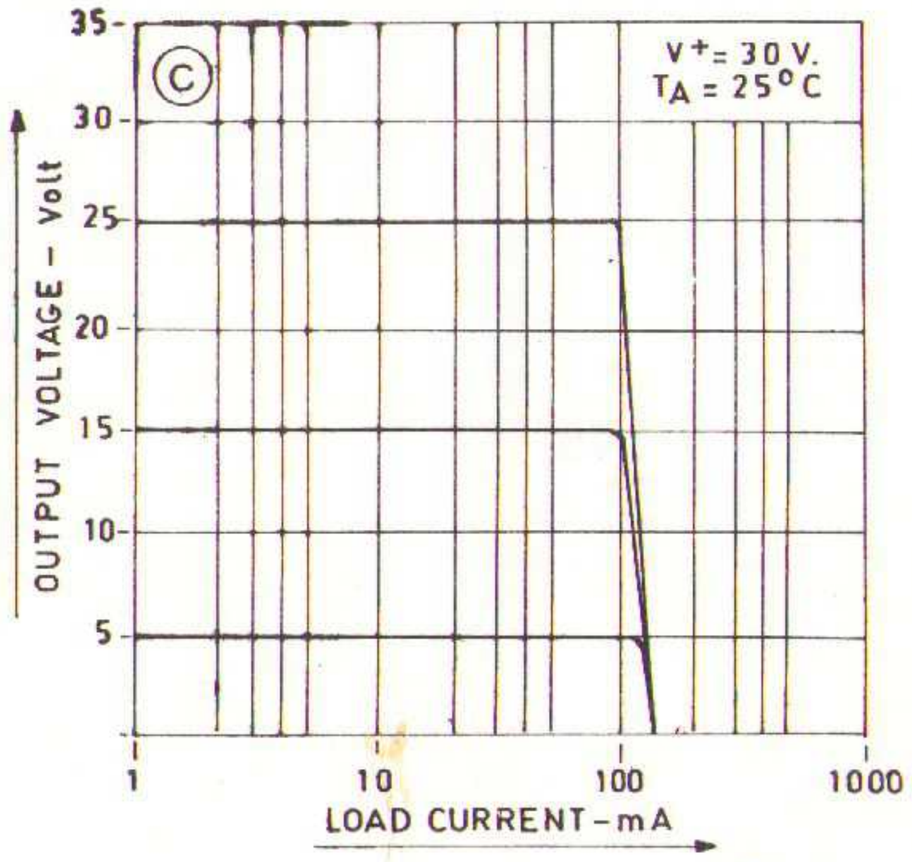
1. It allows greater than 60V output adjustment range.
2. It operates within its specified power supply range.

When operated in this manner, both the regulation (better than 0,01%) and the range of nominal output voltages (up to 250V) are better than standard ground-referenced circuitry. The bootstrap effect is accomplished by the 30V zener diode.This stabilizes the voltage across the operational amplifier at a level that is within the 709's range, and that tracks the output voltage within the control range of the operational amplifier over a wide range of output voltages.

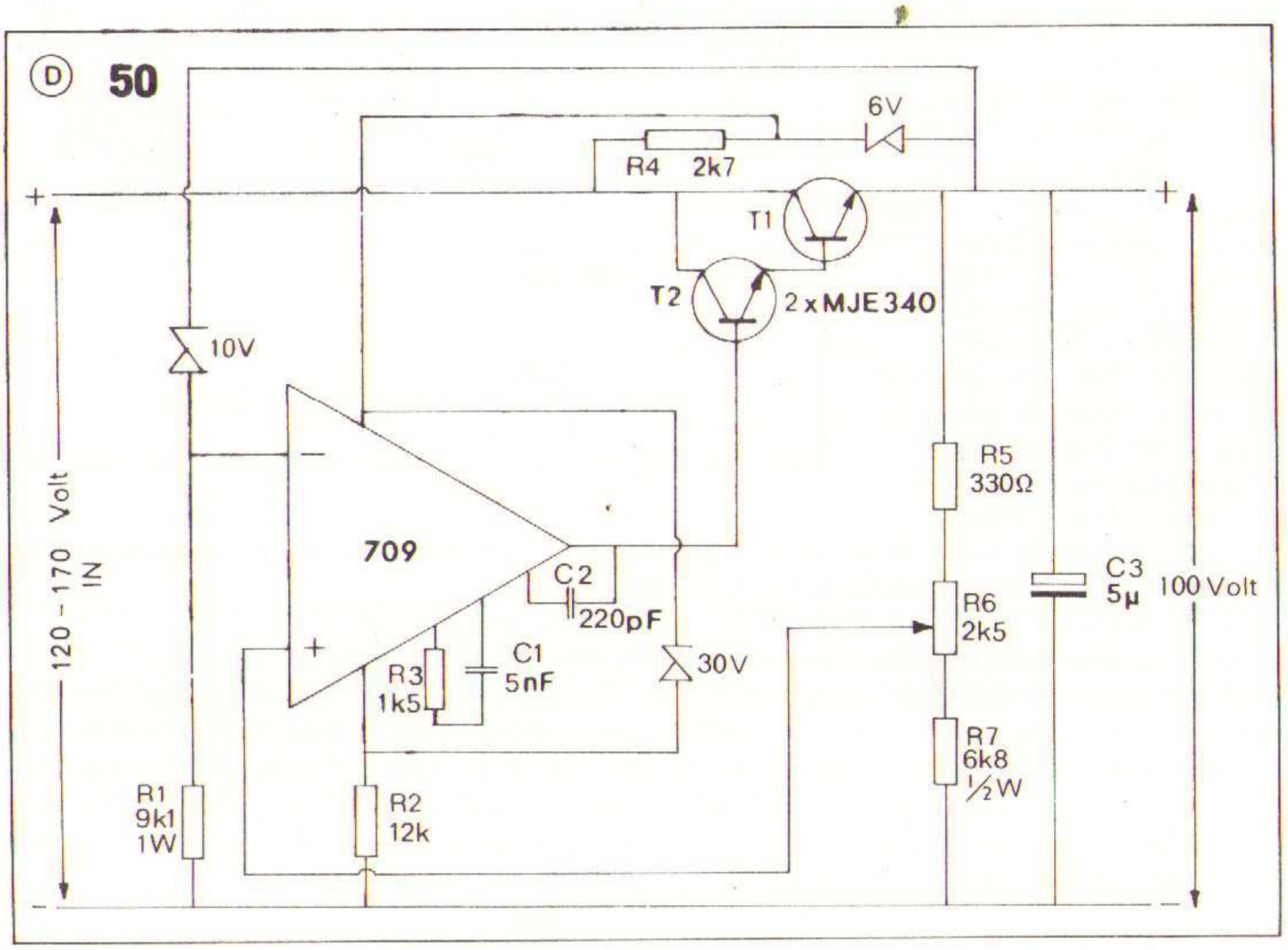
Ⓑ **49**


+30 Volt
R1
10k
C1
5
nF
R8
1k5
D2
D2 = FD300
6V8
R9
10k
R7
6k2
709
R3 1k
T1
2N3054
C2
220pF
T2
BC171B
R4
5,6Ω
R5
10k
UIT
2-5 Volt
100 m Amp.

Ⓒ


V+ = 30 V.
TA = 25°C
OUTPUT VOLTAGE – Volt
35
30
25
20
15
10
5
1
10
100
1000
LOAD CURRENT – mA

Ⓓ **50**


6V
R4 2k7
T1
T2
2 x MJE340
10V
120 – 170 Volt
IN
709
C2
220pF
C1
5nF
R3
1k5
30V
R1
9k1
1W
R2
12k
R5
330Ω
R6
2k5
R7
6k8
½W
C3
5µ
100 Volt

A A N T E K E N I N G E N

N O T E S

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Stuurt U deze dan aan: Van Dam Elektronica, Afdeling: Technische Documentatie 1970, Postbus 3149 te Rotterdam-noord, Holland.

Ook anderen kunnen hieruit iets leren . . . . . ! ! !

van dam
ELEKTRONICA

ECONOMICAL REVERSIBLE DC MOTOR CONTROL

James M. Garrett

For a dc motor to run at a selected constant speed in either direction, its two leads must be supplied with voltage of the proper polarity that is automatically varied as the load changes. This report describes an economical solid-state circuit which regulates a single-polarity dc power source to set the speed and direction of a reversible dc motor regardless of its shaft load (within the rating of the motor).

Since a major cause of concern and expense in such controls is the selection and arrangement of the output transistors, this problem is the primary one discussed here. The output network is two complementary pairs of power transistors from the Texas Instruments series of low-cost, single-diffused, epitaxial-base plastic transistors. Devices from this series have the heat dissipation ratings, secondary breakdown characteristics, complementary features, and high gain which are important in this type of application. This particular circuit, simple in design, may be used without modifications or adjustments. However, its main purpose is not to provide a complete system design but rather to demonstrate a concept of low-cost complementary power transistors used in reversing motor speed controls.

PRINCIPLE OF OPERATION

The circuit (Figure 1) can be used to control several types of motors: permanent magnet, low-voltage universal, or direct current. Likewise, any of several types of tachometer generator may be used. In a given system (with a certain motor and tachometer generator), the control circuit functions as follows: the speed-control potentiometer is set at the position which produces the motor speed desired for some given load. When the load changes, the speed tends to change also——but the control circuit automatically adjusts the voltage supplied to the motor to minimize the speed change. The closeness of this regulation depends partly on the characteristics of the motor and the design of the tachometer generator.

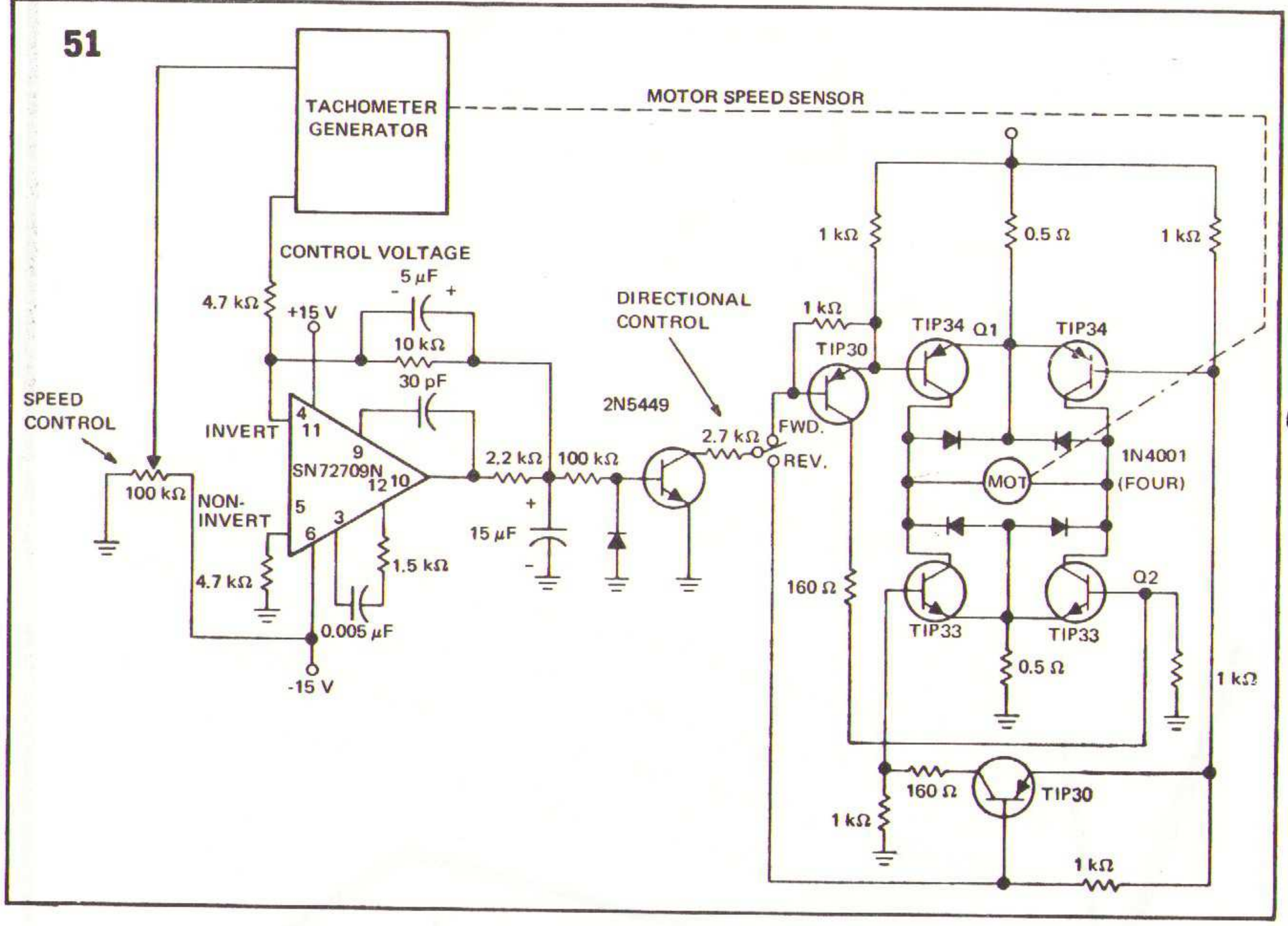


FIGURE 1. Automatic Speed Regulator for a Reversible DC Motor

The function of the tachometer generator is to measure the speed of the motor (regardless of direction), compare it to the desired speed signaled by the potentiometer, and supply a control voltage to the rest of the circuit. This control voltage is zero when the speed is at some value slightly greater than that desired for a given load. As motor speed drops from that excessive value, the control voltage increases in the negative direction. The rest of the circuit serves simply to amplify this control voltage—from zero to line supply voltage. Consequently, both the control voltage and the motor voltage are roughly proportional to load, so that the speed is roughly constant.

At an intermediate amplification step, a single-pole, double-throw switch is located which selects the direction of motor rotation.

DESCRIPTION OF CIRCUIT

The PNP TIP34 (Q1) and the NPN TIP33 (Q2) are placed in series with the motor to control current. The base current of each TIP34 is passed by a TIP30 into the base of a TIP33. This device configuration results in equal output-device dissipation. Each TIP30 is driven by the 2N5449 NPN Silect* device, which in turn is driven by the SN72709N integrated-circuit amplifier, according to the control voltage command.

The gain of the SN72709N and subsequent stages determines the speed regulation precision of the motor. Usable gain, however, is limited by the electrical properties of the motor and speed transducer. A Bodie plot will demonstrate that these properties can produce phase shifts which cause system oscillations if the system gain is too great.

Figure 2 shows the power dissipation that the TIP33 output devices can tolerate under dc conditions. Any operating point below and to the left of this line is in the rated "safe operating region" of the device. At reduced speed settings, high power dissipation can occur in the output complementary pairs. To demonstrate the magnitude of this dissipation, assume the power source (V_{CC}) is 24 V dc. Then suppose that a 5-A, 24-V dc motor is operating at reduced speed at 4 V and that at this low voltage the motor draws only 4 A. Power dissipated by each output device is $V_{CE}\ I_C = (24\ V - 4\ V)\ (4\ A) = 80\ W$.

It becomes obvious that high dissipation can be encountered and that this heat must be removed by proper heatsinking. With the TIP33 and TIP34 devices (each capable of dissipating 80 W), total dissipation as high as 160 W could result if two devices were mounted on one heatsink. The maximum safe dc operating area also indicates what V_{CC} level can be tolerated at all possible current levels. Figure 2 indicates that for V_{CE} values above 30 V, the dc power dissipation rating of the device is reduced below 80 W as shown.

Diodes are placed across all the power output devices to protect the transistors against inductive "kickbacks" when the motor is being reversed.

The purpose of the SN72709N is to provide higher system gain. To simplify the control circuit, (where speed control feedback is not required) the SN72709N can be excluded. In such case, the base of the 2N5449 can be driven directly to control the motor.

Figure 3 shows the effectiveness of the illustrated control circuit in maintaining motor speed under changing load. The top curve represents the motor behavior without feedback, while the other curves indicate close speed regulation until they reach the overload point of the motor. These curves were made up for a particular motor; other motor types have slightly different curves but perform approximately the same.

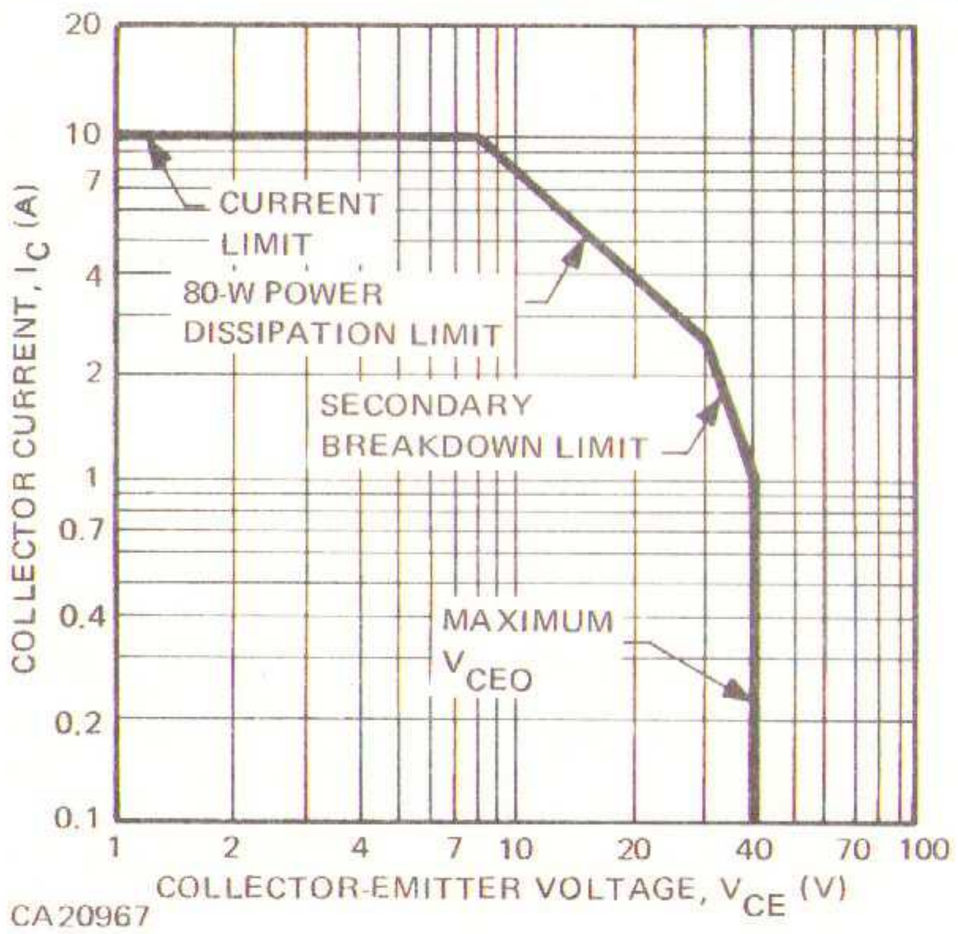


FIGURE 2. Safe Operating Region of TIP33 in DC Operation, Case Temperature ≤ 25°C

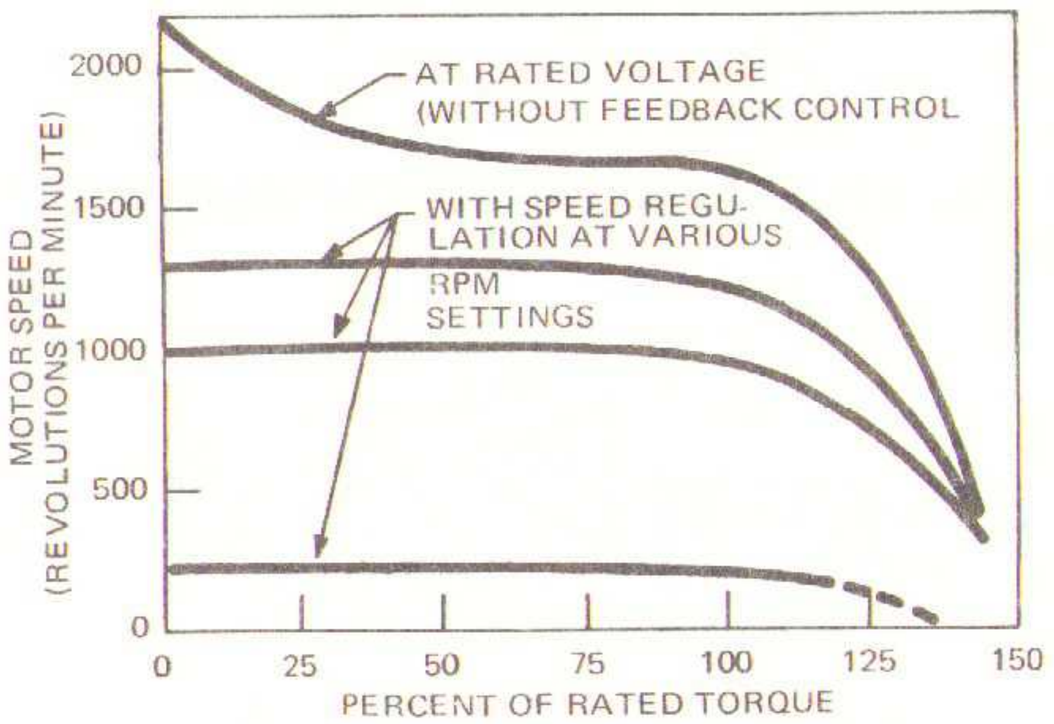
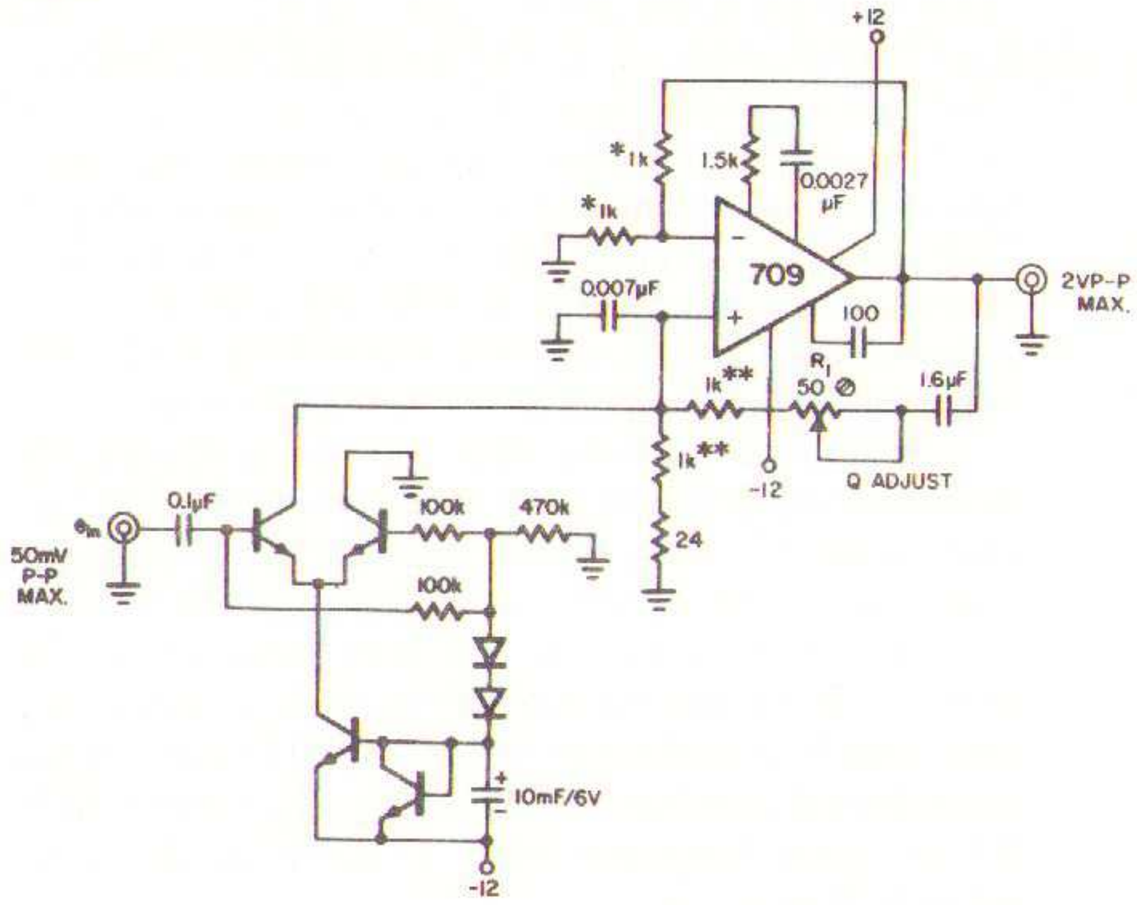


FIGURE 3. Effectiveness of Figure 1 Circuit in Controlling Speed of a 1/3-hp 27-V DC Motor

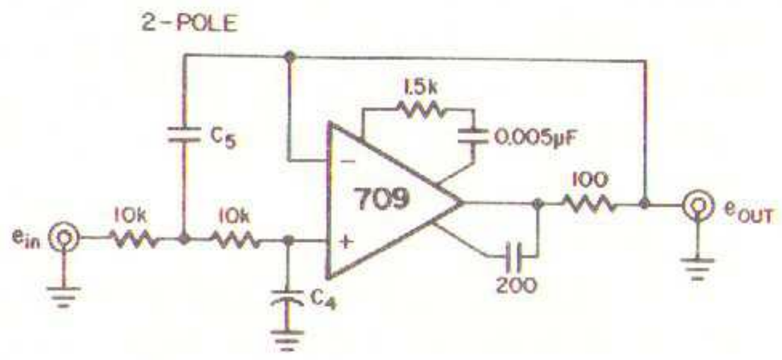
* Trademark of Texas Instruments

ACTIVE BANDPASS FILTER, ADJUSTABLE Q
52

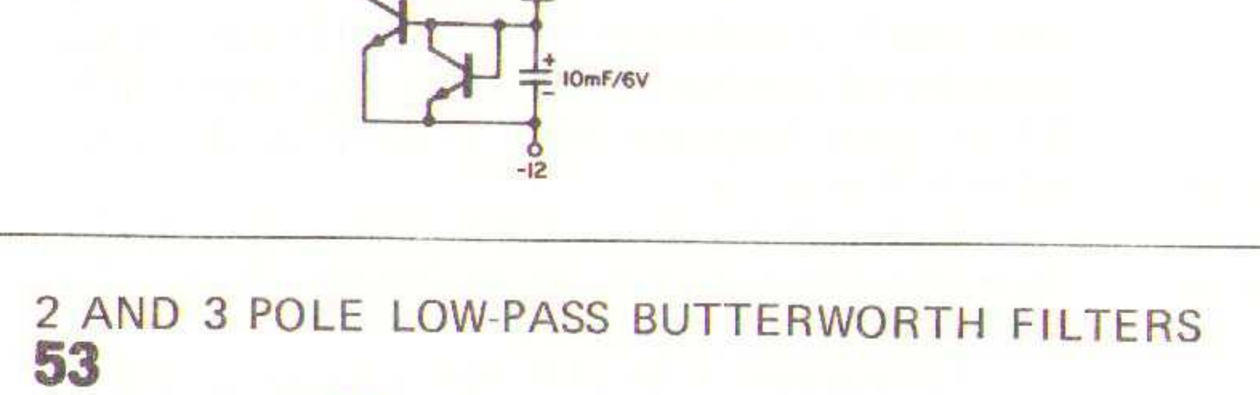


Notes:
1. Center frequency with components shown ≈ 1.5 kHz.
2. Q may be adjusted by means of R_1: Q's of 100 are stable.
3. Center frequency gain ~ 40 at Q = 100.
4. * and ** matched pairs, to 1%.

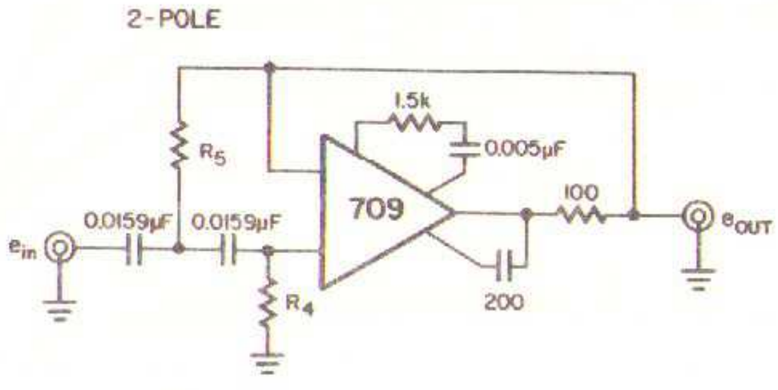
2 AND 3 POLE LOW-PASS BUTTERWORTH FILTERS
53



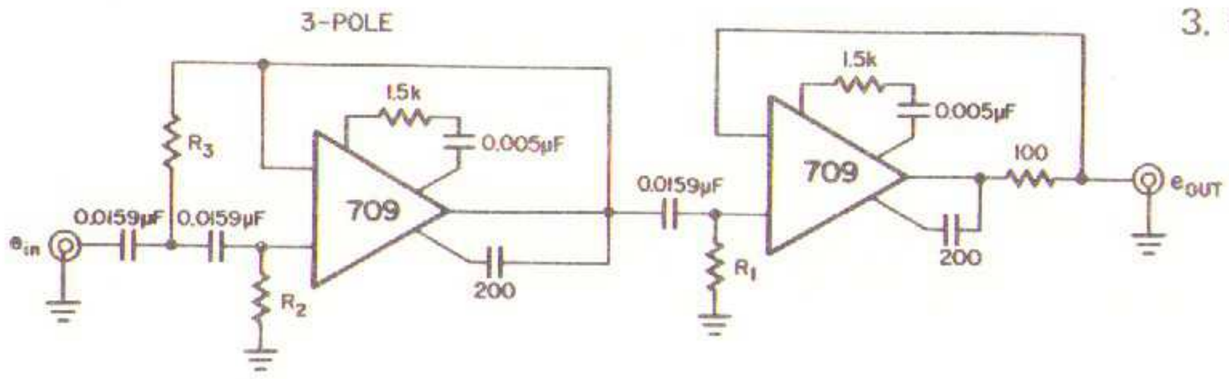
Notes:
1. $C_5 = \sqrt{2}C_1$; $C_4 = \frac{1}{\sqrt{2}} \cdot C_1$; $C_3 = 2C_1$; $C_2 = \frac{1}{2} C_1$
2. At f_o = 1 kHz, C_1 = .0159µF
3. Undistorted output limitation is: $e_{out_{peak}} \cong \frac{30}{f_{kHz}}$
4. DC return path is required for e_{in}.



2 AND 3 POLE HIGH-PASS BUTTERWORTH FILTERS
54

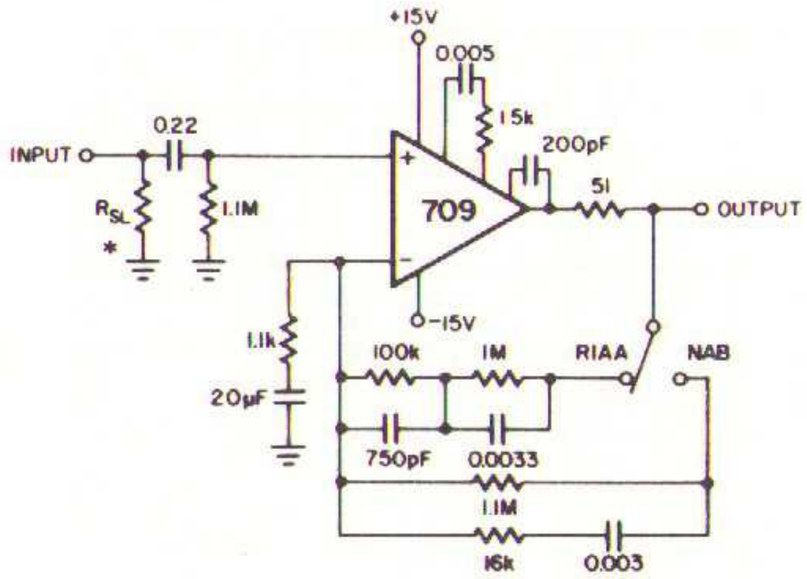


Notes:
1. $R_5 = \frac{1}{\sqrt{2}} R_1$; $R_4 = \sqrt{2}\ R_1$; $R_3 = \frac{1}{2} R_1$; $R_2 = 2R_1$
2. At f_o = 1 kHz, R_1 = 10k.
3. Undistorted output limitation is: $e_{out_{peak}} \cong \frac{30}{f_{kHz}}$



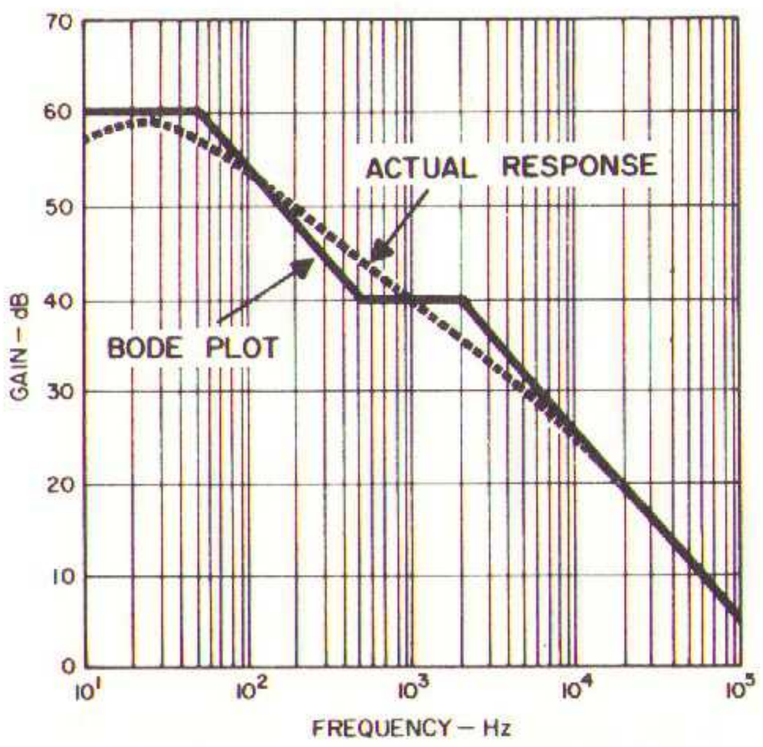
PREAMPLIFIER – RIAA/NAB COMPENSATION

55

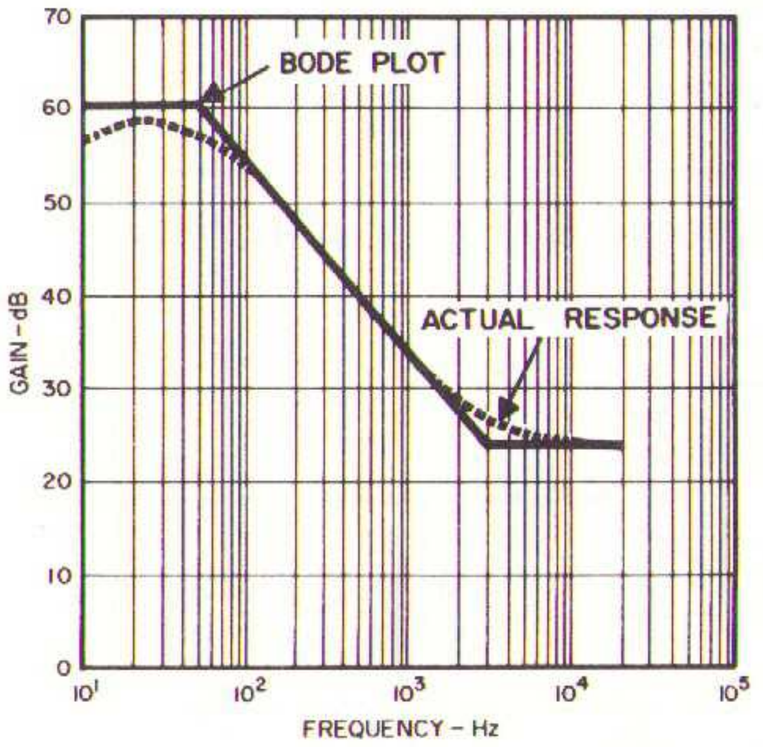


* Select to provide specified transducer loading.

Output Noise ≅ 0.8mV rms (with input shorted)



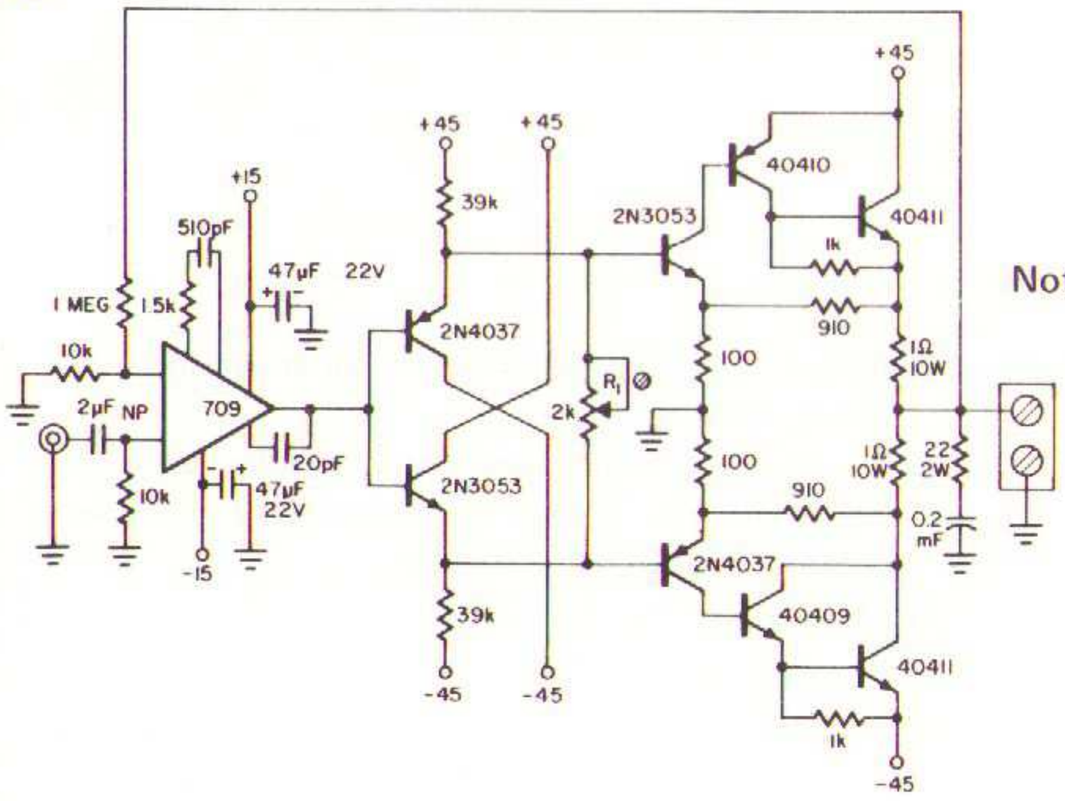
Bode Plot of RIAA Equalization and the response realized in an actual circuit using the 709.



Bode Plot of NAB Equalization and the response realized in the actual circuit using the 709.

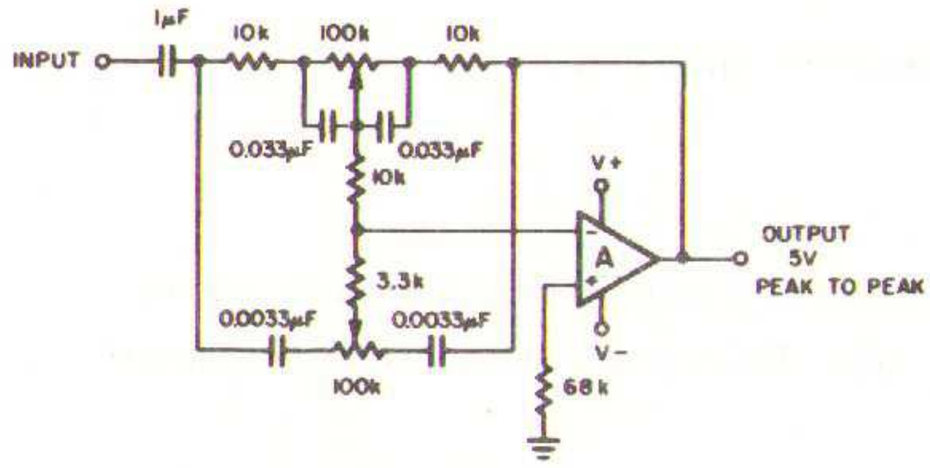
100W RMS AUDIO POWER AMPLIFIER

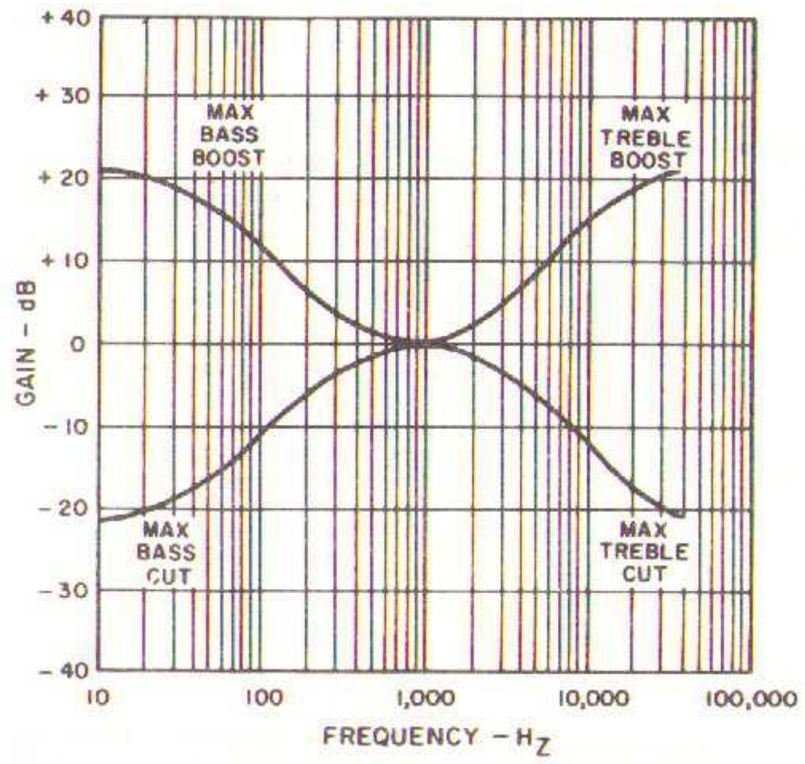
56



Notes:
1. Set R_1 to 0Ω at initial turn-on.
2. Adjust R_1 for 150mA collector current at no signal.
3. 1 kHz distortion is less than 0.1% at 70W.
4. P_{out} is for 8Ω load: For 16Ω load, P_{out} = 50W.

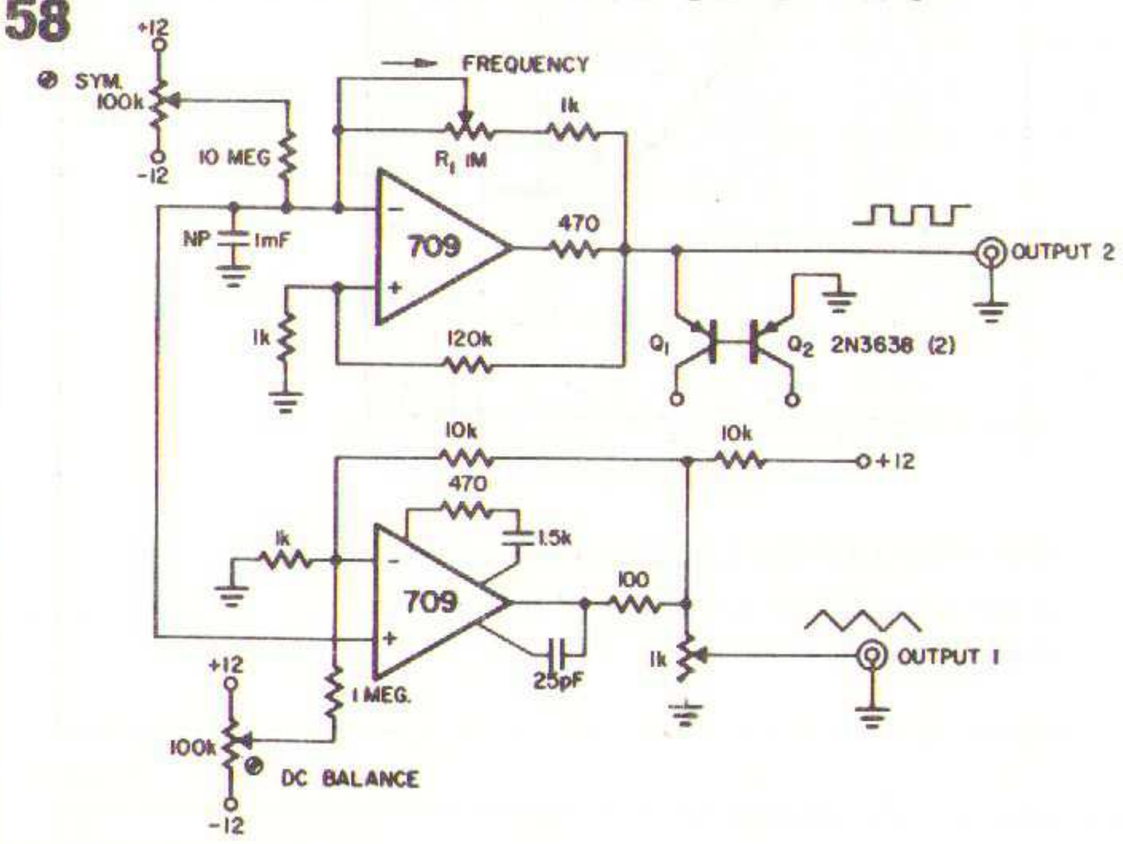
TONE CONTROL CIRCUIT FOR OPERATIONAL AMPLIFIERS
57





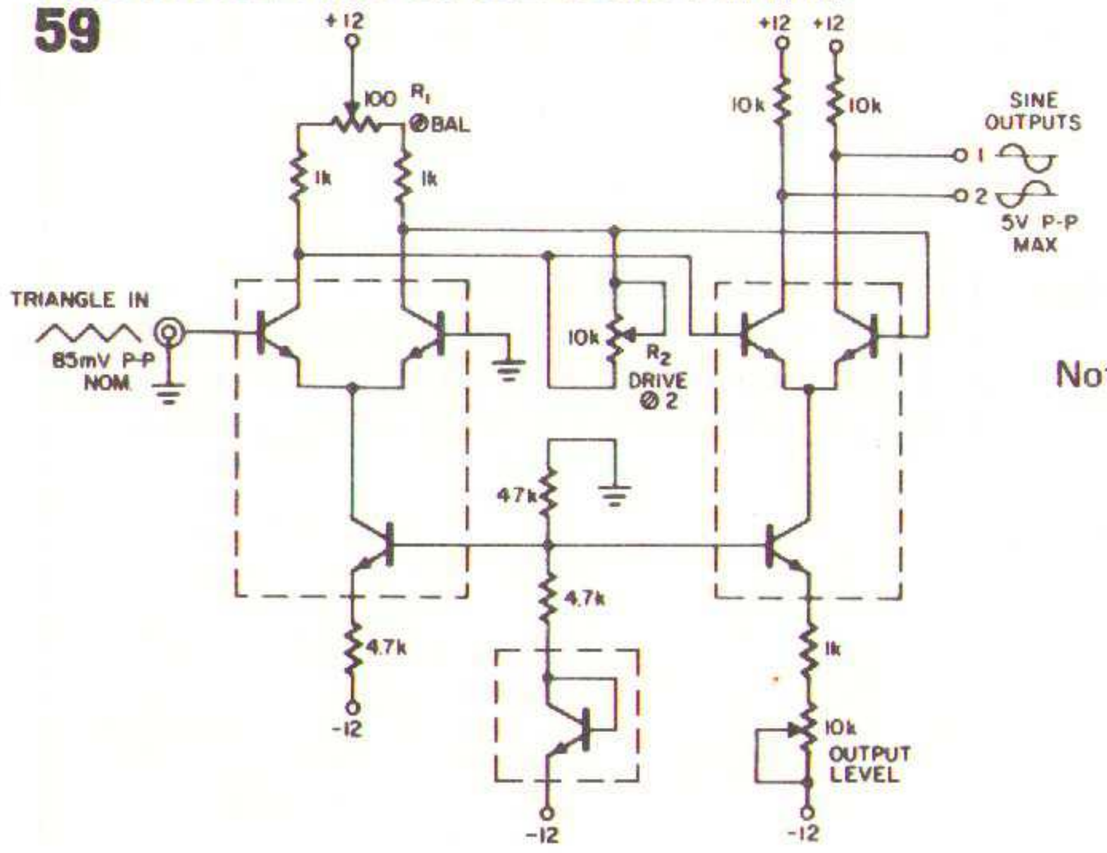
Notes:
1. Amplifier A may be a 709 Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over Frequency – 1kHz.
3. Bass Boost – 20dB at 20Hz
   Bass Cut – 20dB at 20Hz
   Treble Boost – 19dB at 20kHz
   Treble Cut – 19dB at 20kHz

TRIANGLE/SQUARE WAVE GENERATOR
58



Notes:
1. R_1 is log taper.
2. Q_1 and Q_2 selected for 20mV match.
3. Symmetry is better than 1%, 30Hz – 25kHz.

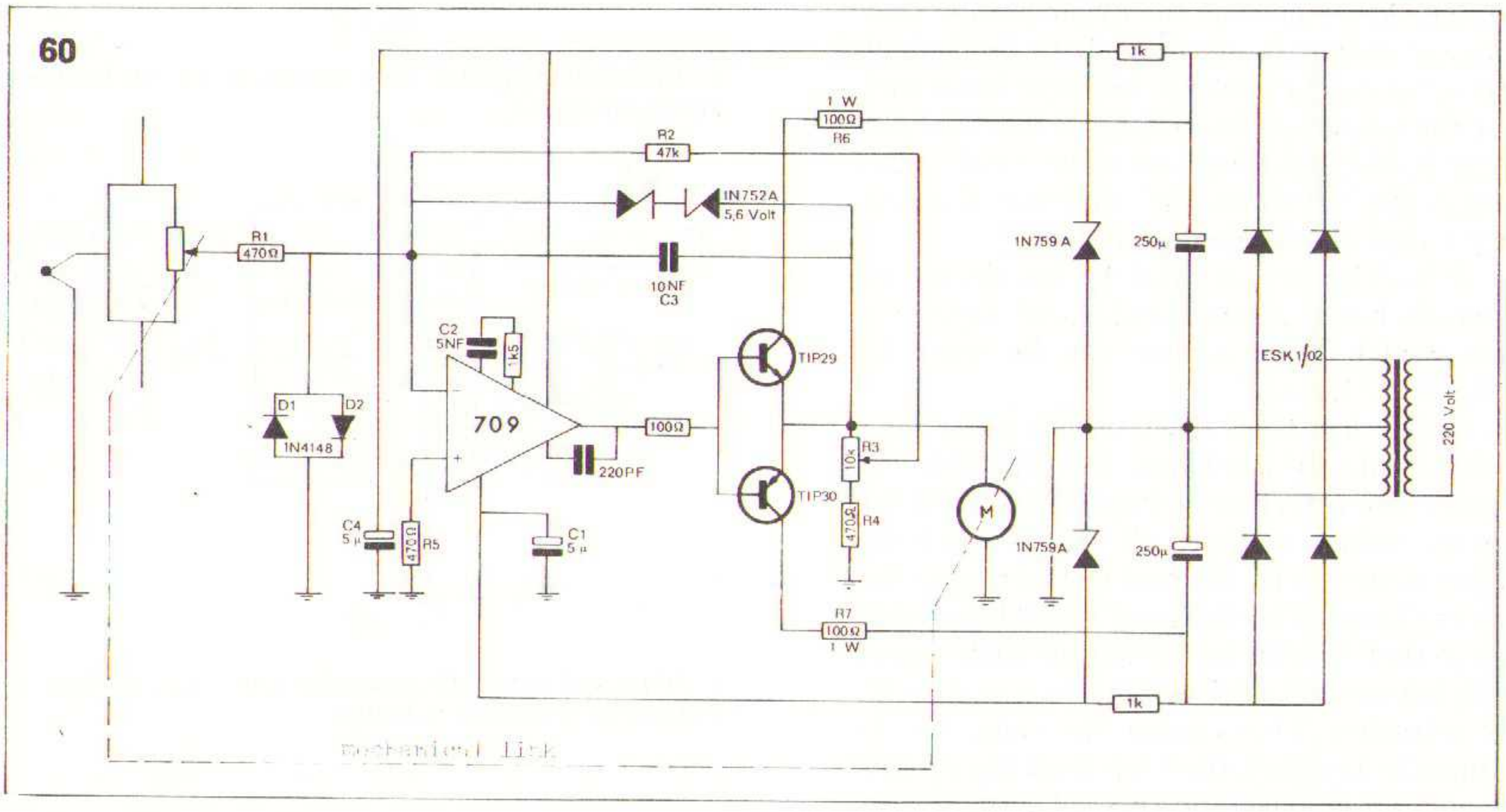
TRIANGLE/SINE WAVE CONVERTER
59



Notes:
1. Circuit may be used with the square/triangle generator, shown separately.
2. R_1, R_2, and input level may be adjusted to give less than 2% T.H.D. at output using Hewlett-Packard 333A Dist. Analyzer.
3. IC: CA 3046 (2x).

SERVO - AMPLIFIER

Used for driving a 6V low power DC motor in a servo-mechanized thermo-couple thermometer

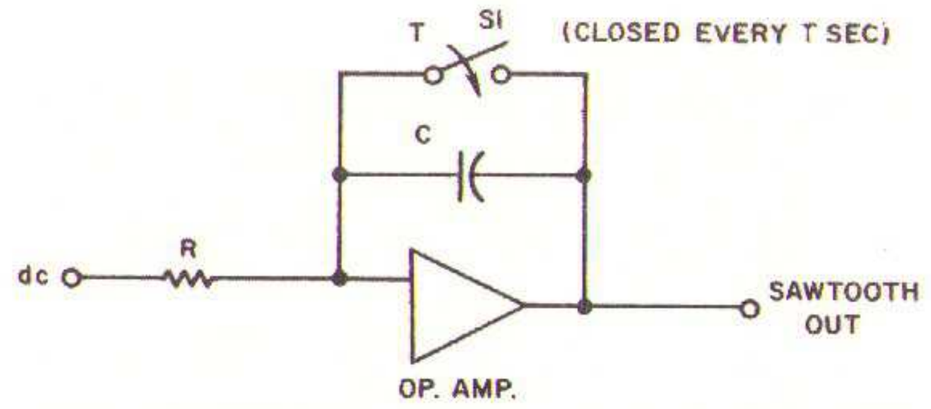


1. Purpose: Driving a low power D.C. motor from the low D.C. voltage issued from a thermocouple associated with a servo mechanized null-bridge.
2. Operation:
   2.1 Thermocouple and bridge.
   They have to be designed by the costumer for the thermocouple characteristics and the temperature scale.
   2.2 Servo amplifier.
   Made with a low drift 709 I.C. amplifier associated with two power transistors TIP 29 and TIP 30 (Texas Instuments) used to provide power to the motor.
   Around this amplifier are:
   a. a resistor network (R1, R2, R3, R4) used to give the optimum gain to the amplifier.
   b. two diodes (D1 and D2) to avoid an excess in voltage accross the amplifier inputs.
   c. a frequency compensating network made of R5, C1, C2 and C3.
   d. in order to protect the servo amplifier against a too high output current (motor stalled) R6, R3 and R7 are used.
   e. The motor used being a 6V type, the amplifier output is limited to ±6,2V ±5% by the use of two 5,6V Zener diodes mounted accross the feed back bridge.
   2.3 Power supply.
   Uses a 127/220V 50Hz to 2 x 15V transformer; the output of which is rectified through a four ESK 1/02 diode bridge and then, filtered by two 250µF 25V electrolytic capacitors. This voltage feeds directly the two power transistors. The power is supplied from this point to the I.C. amplifier through a stabilizing network made of two 1kΩ resistors, two 12V zenerdiodes and two 5µF ≥15V solid tantalum capacitors. These capacitors MUST be wired as close as possible to the IC terminals.

Improved sawtooth generator has grounded reference point

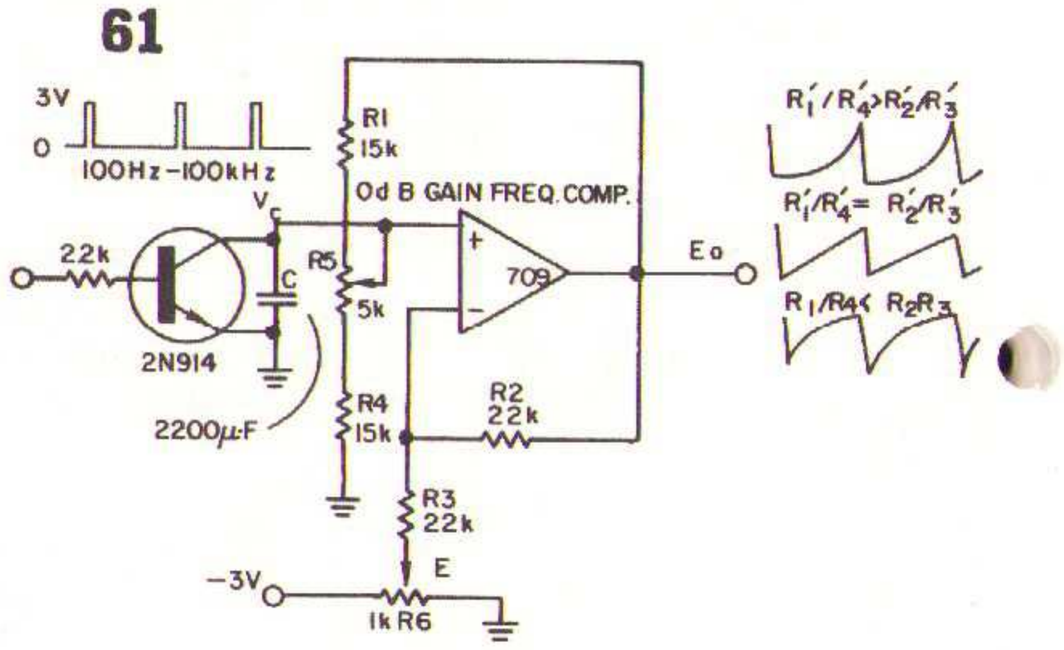
Problems associated with sawtooth generators using operational amplifiers stem from difficulties with resetting. An improved circuit eliminates this problem through the use of a ground-referenced capacitor yet allows high linearity of the classical integrator.

The classical integrator configuration is shown in Fig. 1. The approach has the disadvantage that the discharge switch, S_1, is difficult to implement since the capacitor is floating between input and output of the amplifier. Switching in this configuration may reduce linearity and make it quite difficult electrically to change the capacitor if a new frequency range should be desired.



1. **Classical integrator** has capacitor that floats between input and output.

These difficulties are avoided by the design in Fig. 2, which has a ground-referenced capacitor and reset switch. This circuit can be reset by standard 5-V IC logic.



2. **Improved sawtooth generator** has capacitor that is referenced to ground potential.

If the circuit has been reset with a pulse long enough to completely discharge the capacitor, V_c will be zero. The reference voltage E (0 to –3 V) produces an output voltage, $-R_2/R_3E$, which divides across resistors R_1, R_4, and R_5 and causes the capacitor to charge. The charging would be asymptotic except that V_c adds to the output with a gain of 2 and is fed back by a 0.5 voltage divider with R_5 properly adjusted. This causes the capacitor to charge linearly. In effect, the drop from the capacitor to the output is fixed, and this holds the charging current constant between reset pulses.

$$E_o(s) = \frac{R_2+R_3}{R_3} V_c(s) - \frac{R_2}{R_3}\frac{E}{S}, \text{ neglecting R6}$$

$$\text{where } V_c(s) = \frac{R'_4\, E_o(s)}{R'_1\, R'_4\, CS + R'_1+R'_4},$$

$$R'_1=R_1+aR_5,\ R'_4=R_4+(1-a)R_5$$

$$\text{Then: } E_o(s) = \frac{-R'_1R_2R'_4\, E\, C\, S-R_2\, E\, R'_1-R_2R'_4\, E}{S\left(S + \dfrac{R'_1\, R_3-R_2R'_4}{R'_1R_3R'_4C}\right) R'_1R_3R'_4C}$$

$$\text{If } R'_1R_3-R_2R'_4 = 0 \text{ or } R'_1/R'_4 = R_2/R_3$$

$$E_o(s) = \frac{-R_2E}{R_3S} - \frac{R_2(R'_1+R'_4)E}{R'_1R_3R'_4CS^2}$$

$$E_o(t) = \frac{-R_2E}{R_3} - \frac{R_2(R'_1+R'_4)\ (E)t}{R'_1R_3R'_4C},\ 0<t<T$$

Thus if R_5 is adjusted to give $R'_1/R'_4 = R_2/R_3$, a perfect linear ramp is generated. If $R'_1/R'_4<R_2/R_3$ or $R_1/R_4 > R_2/R_3$ a negative or positive exponential is generated respectively. Adjusting R_6 or E controls the output amplitude.

If the feedback is greater than 1, the capacitor voltage V_c adds increasingly to the charging rate, and the output takes off with a positive exponential. When the feedback is less than 1, V_c adds decreasingly to the charging rate, and the output is a negative exponential.

Changing the polarity of E changes the polarity of the ramp, but with the circuit shown only a –1-V peak-to-peak ramp can be generated. The positive ramp amplitude is limited only by the operational amplifier signal swing. If a more negative ramp is desired it is only necessary to keep the transistor base at +3V in the ON state and negative with respect to the ramp in the OFF state. Note that if the unity feedback condition exists, the amplifier theoretically exhibits an infinite input impedance.

The actual generator output is a dc level summed with the sawtooth. Frequency response of the amplifier limits the high-frequency output to 100 kHz, but a good sawtooth can be taken directly from the capacitor up to several megahertz. A larger capacitor will reduce the low frequency limit, but a longer reset pulse is then required to completely discharge the capacitor. It is suggested that the transistor be connected directly across the capacitor with a single common ground wire to reduce ground transients during the discharge cycle. Although the circuit requires the setting of a potentiometer, the ground-referenced capacitor more than compensates for this disadvantage. All parts used are standard 5% components, and the uA709 was operated with zero dB compensation from ± 15-V supplies.

Digital-to-analog converter is fast and simple

The high-speed digital-to-analog converter (see figure) can convert a digital signal of as much as 10-MHz rate to either a positive or a negative analog signal.

Each bit of the binary-coded input is applied to the base of the transistor switches *Q1*, *Q2*, *Q3*, normally biased on ($\bar{A}$=1). When the transistor switch is turned off by a bit ($\bar{A}$=0), the reference voltage, E_{REF}, is summed through the amplifier. The values of the input resistances (*R8* + *R2*) are chosen so that each allows an amount of current flow that is proportional to the weight or significance of its respective binary digit.

Resistances *R2*, *R4* and *R6* are selected to establish the maximum current through the transistor switch. Resistor *R11* is adjusted to compensate for the saturation voltage drop across the switches.

Amplifier *Z1* is a standard wide-band summing amplifier. Frequency compensation network, *R13* and *C5*, is selected for maximum bandwidth. Emitter-follower *Q4* reduces output loading and allows a full 4 V negative swing. It should be noted that the output is independent of the absolute value of the input logic levels.

The values of *R10*, *R9* and *R8* are computed as follows. Let $E_{out(max)} = 4$ V. This value corresponds to the binary number 111, or the decimal number 7. If *C* is the least significant bit, then

$C = E_{out(max)}/N = -4/7 = -0.57$ V,

$B = 2C = -1.14$ V

$A = 4C = -2.28$ V.

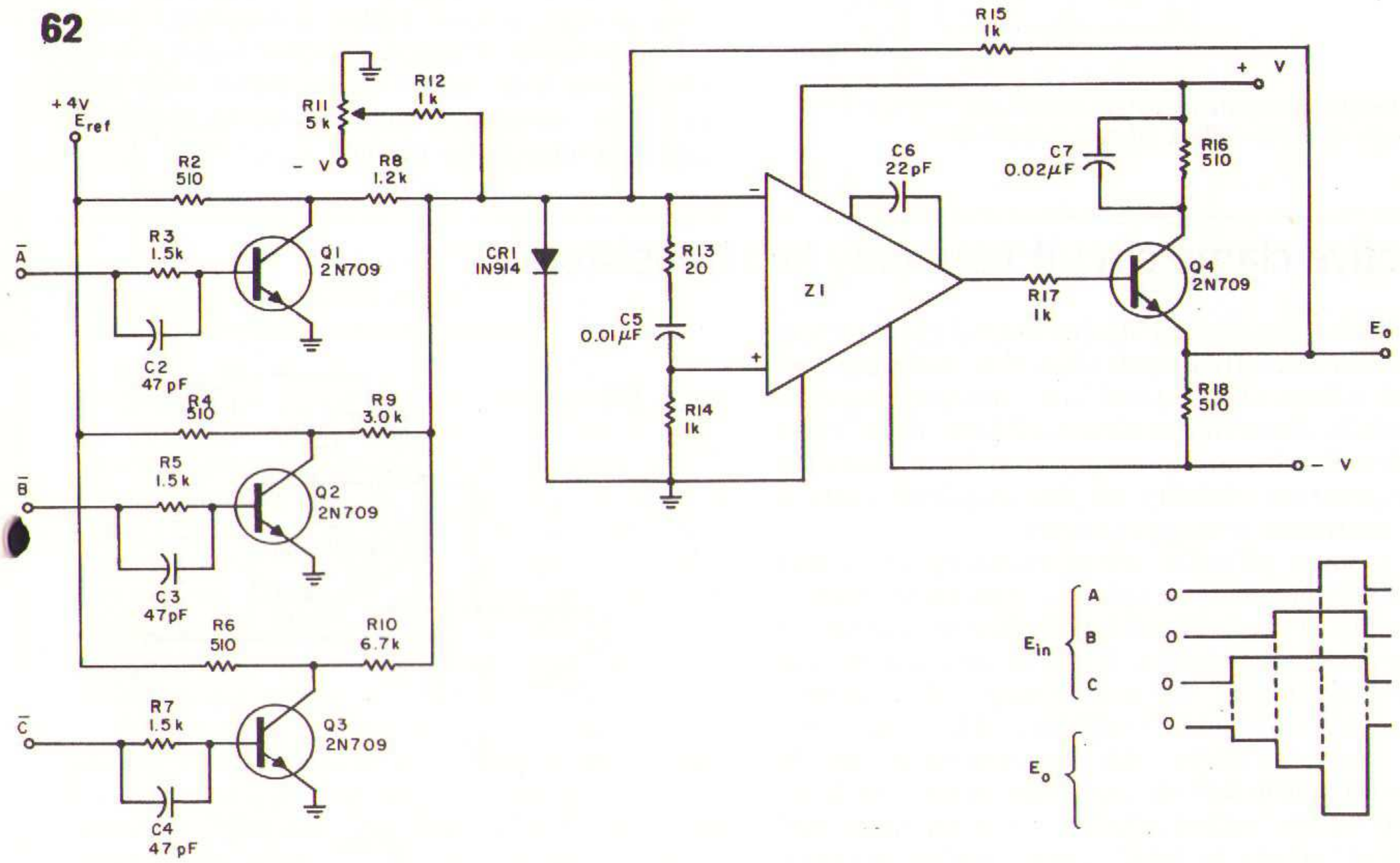
R10, associated with *C*, is then

$E_o/E_{in} = R15/R6 + R10$

$R10 = 6.7$k

R9, associated with *B*, is 3k.

R8, associated with *A*, is 1.2k.



Digital-to-analog converter can accept digital data at up to 10 MHz rates.

Inexpensive circuit generates precision unipolarity output

Many circuit variations exist for generating a precision dc output voltage of one polarity for either polarity of dc input voltages. The circuit described here is simple and uses fewer components than other versions.

One transistor and one carbon resistor are used in addition to the operational amplifier and its gain determining resistors, R_1 and R_2, to achieve 0.02% performance. For positive input voltages ($+E_{in}$), the output of K_1 is negative, thus causing CR_1 to conduct and biasing Q_1 off through R_3.

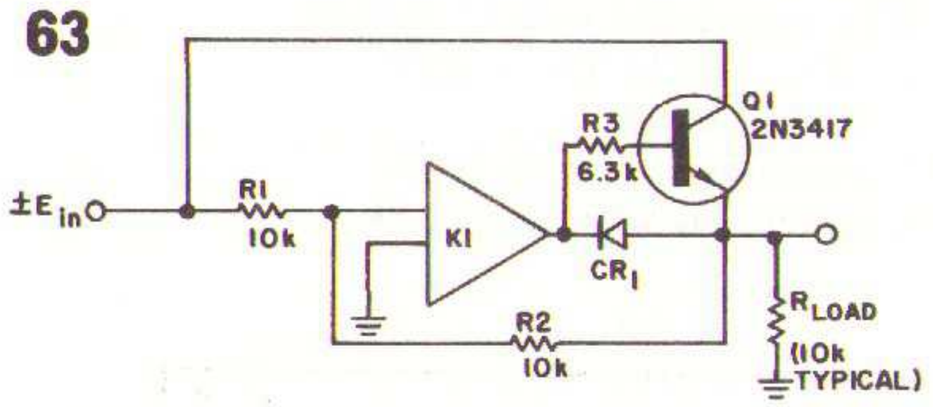
Since the feedback is sensed on the output side of CR_1, the offset voltage across CR_1 does not affect the linearity as long as K_1 has a high open-loop gain ($> 10{,}000$). When the input signal becomes negative ($-E_{in}$), the output of K_1 becomes positive. This reverse biases CR_1 and causes *Q1* to saturate in the inverted-mode (base current flows through R_3 and the base-collector path of *Q1*).

When *Q1* saturates, E_{out} becomes nearly equal to $-E_{in}$ in both polarity and magnitude. *Q1* becomes heavily saturated for a very small value of E_{in} due to the high open-loop gain of K_1. Typically, for a 2N3417, offset voltages near zero are only 0.3 mV, and only a few mV for several milliamperes of load current. R_1 can be adjusted to match the gain of the + input voltages to the – input.

The switching current that flows through R_3 and *Q1* into the source of $+E_{in}$ must be considered. However, the extra loading on the source can be very small if the application will permit large values for R_1, R_2, R_3 and R_{load}. Normally, the circuit would be driven by a preamplifier, which would satisfy the loading requirements.

Another useful feature of the circuit is that the large step voltage that appears as the output of K_1 may be used to drive a polarity-indicating circuit. This permits a very simple autopolarity analog meter to be constructed. Another feature is that the circuit will rectify an ac signal with great precision. Sinusoidal voltages can be handled by adding a filter to the output.

63



Precision unipolarity output circuit operates by either saturating or cutting off output transistor.

Active clamp circuit uses only two transistors

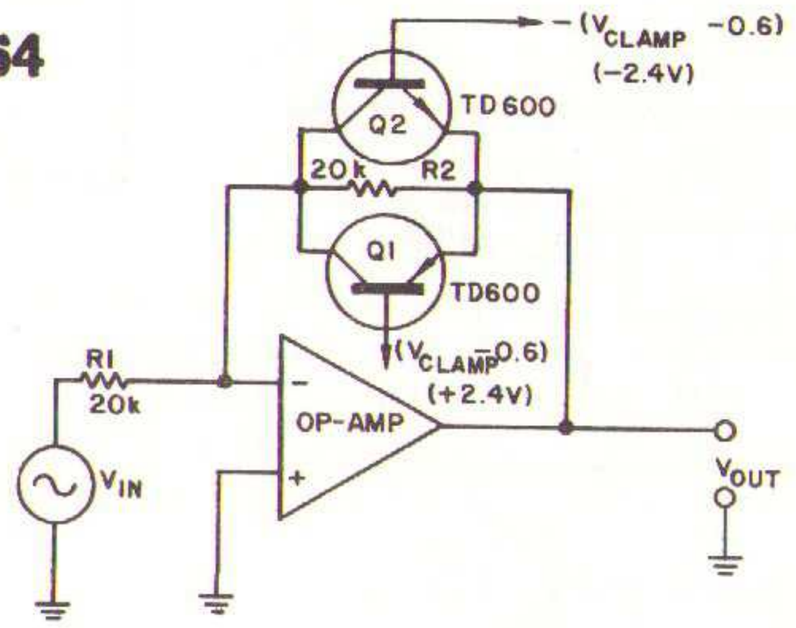
Back-to-back zener diodes around the feedback resistor are often used when the maximum output voltage of an operational amplifier must be limited. Zener diodes have poor breakdown knees below 6 volts, are quite noisy, and can upset the temperature stability of the amplifier because of increased leakage currents.

A more efficient active clamping circuit (a) can be formed by connecting two transistors in parallel with the feedback loop, and biasing the transistors to conduct at the desired output voltage. *Q1* and *Q2* change the amplifier characteristic from linear to logarithmic. The logarithmic connection ensures that the op-amp inside the feedback loop will remain active during the duration of the output overload. The amplifier will quickly return to linear operation after the overload has been removed.

The recovery time of this circuit was measured by inserting a small-amplitude 500-kHz signal in series with an overdriving 10-volt input pulse. The output response indicated that the amplifier returns to linear amplification of the 500-kHz signal approximately 0.5 μs after the overload condition is removed.

Loop transmission of the op-amp must be compatible with the additional gain contributed by the transistors during the clamped period. Further, the BV_{EBO} rating of the transistors cannot be exceeded.

64

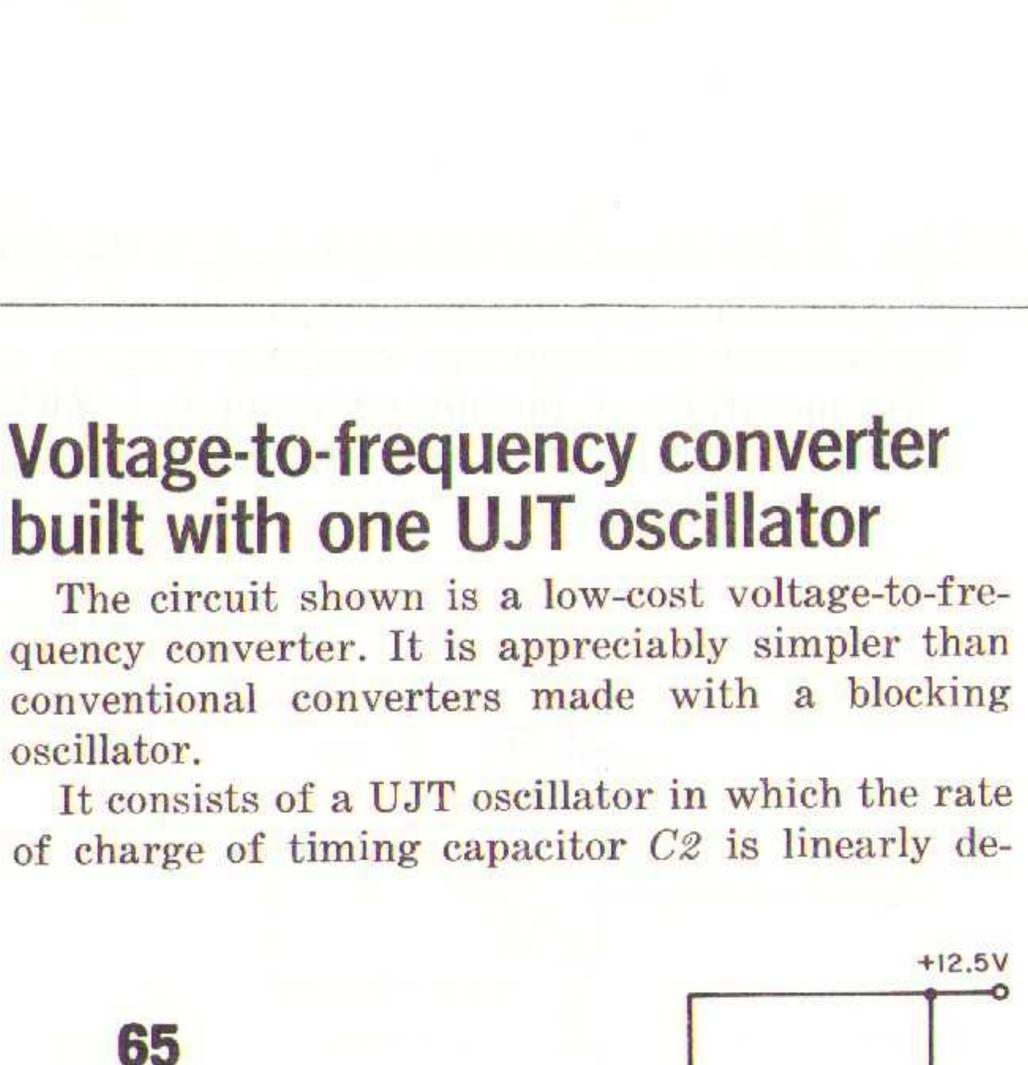


Active output voltage clamp (a) uses two transistors to achieve desired transfer characteristic (b).

Voltage-to-frequency converter built with one UJT oscillator

The circuit shown is a low-cost voltage-to-frequency converter. It is appreciably simpler than conventional converters made with a blocking oscillator.

It consists of a UJT oscillator in which the rate of charge of timing capacitor *C2* is linearly dependent on the input signal voltage. The charging current is set by the voltage across resistor *R5*, which is accurately controlled by the amplifier.



Two decades of frequency range are obtained with this simple VCO (voltage-controlled oscillator).

The range of permitted charging currents is limited by the peak point and valley currents of the UJT. Provided transistor *Q1* has a gain of at least 200 over the charging-current range, linearity is limited by the leakage current of the UJT (effectively reduced by diode *D1*) and the oscillator's minimum duty cycle.

The amplifier is selected to give the required gain at the appropriate input impedance. The combination *R4C1* is used to limit the high-frequency response of the amplifier. The Zener diode is used to adjust the peak-point voltage of the UJT within the output voltage range of the amplifier.

Since the amplifier output is taken with respect to the positive supply, the over-all performance depends on the supply stability. Assuming a typical regulated transistor power supply and the components indicated, however, linearity is better than ±0.5% over a frequency range of two decades, for a signal range of 0 to 1 volt. The temperature coefficient is typically 0.05/°C from 10° to 40°C.

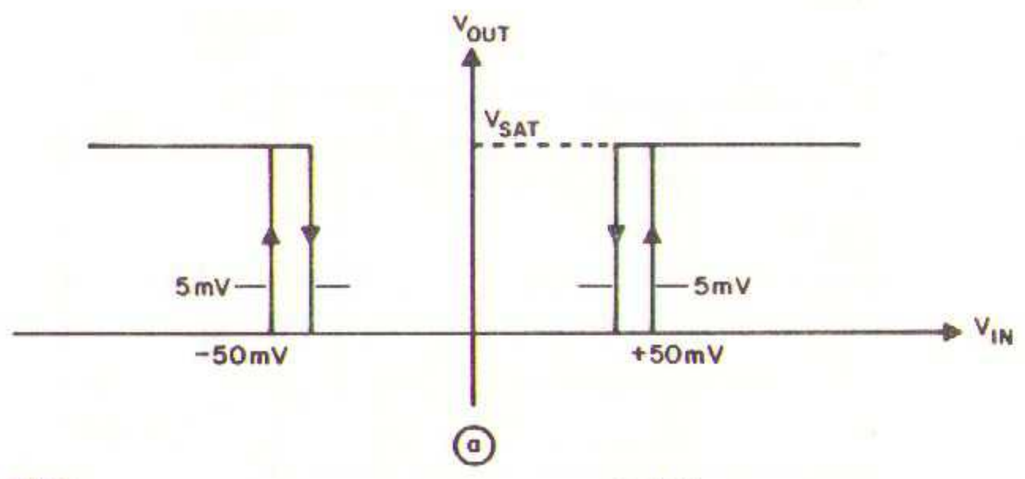
IC window discriminator has predetermined hysteresis

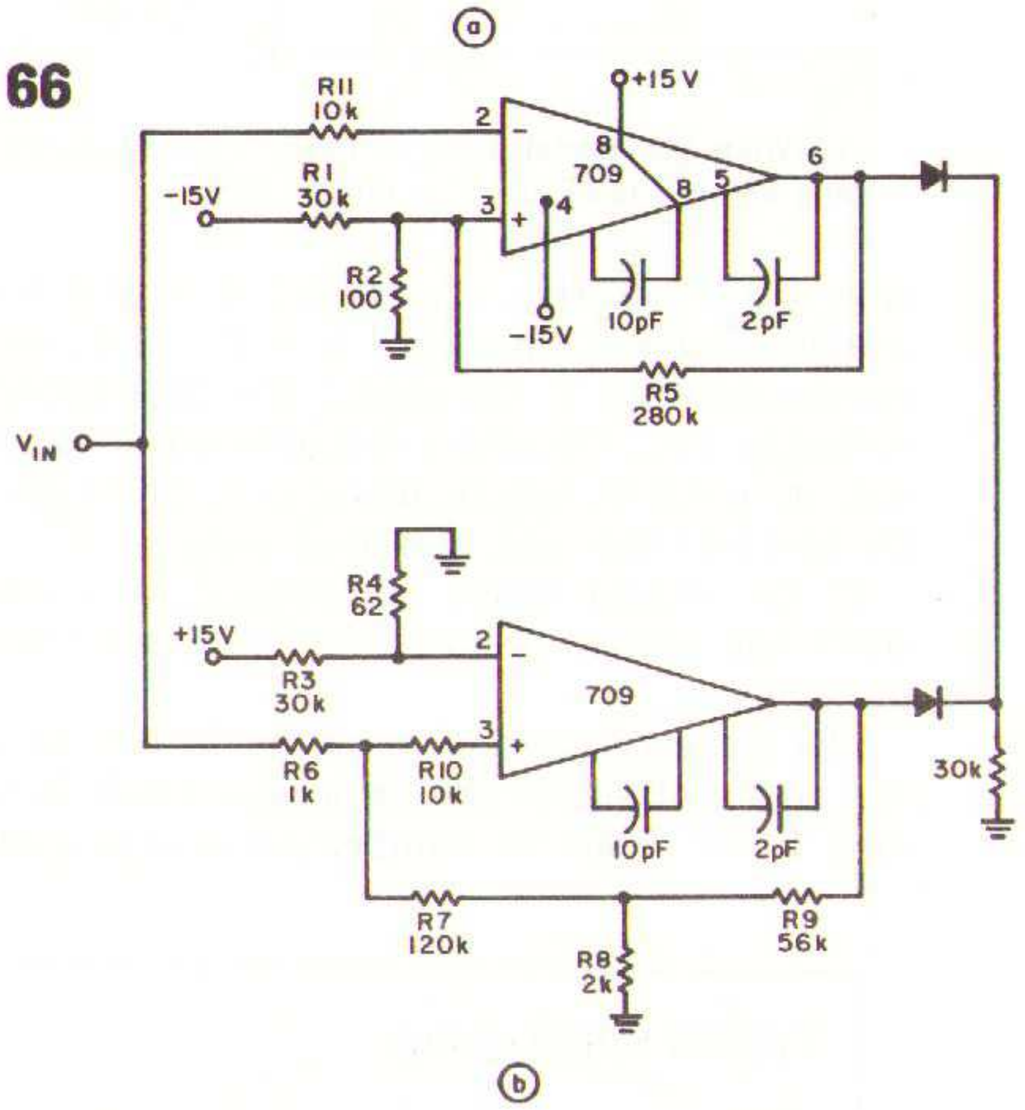
The input-output characteristic shown in Fig. 1a is obtained with the circuit of Fig. 1b. It uses two IC operational amplifiers in positive feedback connection.

Both the positive and negative switching levels and hysteresis can be varied over a wide range by selecting external resistors.

The ratios $V^-_{ref}\ R2/(R1+R2)$ and $V^+_{ref}\ R4/(R3+R4)$ determine the level of detection V^+_{ref} and V^-_{ref} denote negative and positive reference voltages, respectively.

The ratios $V_{out(sat)}R2/(R2+R5)$ and $V_{out(sat)}$





Window discriminator can be adjusted over a wide range of values by selecting external resistors.

$R6/(R6+R7)\,R8/(R8+R9)$ determine the hysteresis.

With the values shown, the detection levels are ±50 mV and the hysteresis is 5 mV.

IC voltage switch is digitally activated

Here is a circuit that provides two output voltages within the range of +0.1 to +10.0 V on receipt of input commands from either TTL or DTL logic.

Applications include digital IC testing, where programmable low and high voltages are required. It should be noted, though, that applications are not limited to digital circuits but include any situations where two or more voltages are to be controlled by digital logic.

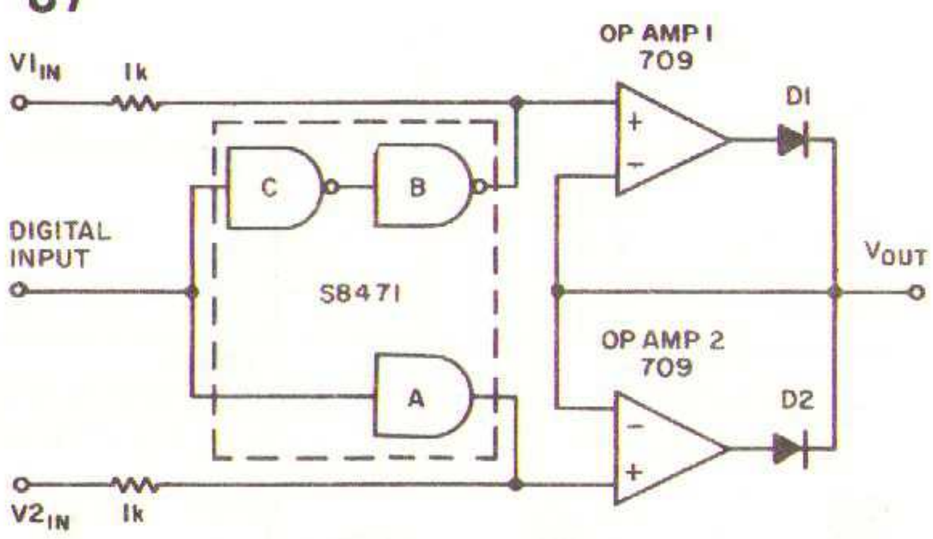
The circuit uses two IC op amps and one digital IC (Fig. 1). The NAND gates have "bare" collector outputs, which represent either a very high or low impedance, depending upon the digital input. The op amps provide effective buffering between the input and output.

In operation, if the digital input is a ZERO the output of gate *A* is high and the input to op amp *2* is $V2_{in}$. Also, the output of gate *B* is low and the input of op amp *1* is a V_{ce} (*sat*) or approximately 0.1 V. Op amp *2* will thus force the output to $V2_{in}$. Op amp *1* will attempt to force the output to 0.1 V, but in doing so it will turn off *D1* and be taken out of the circuit.

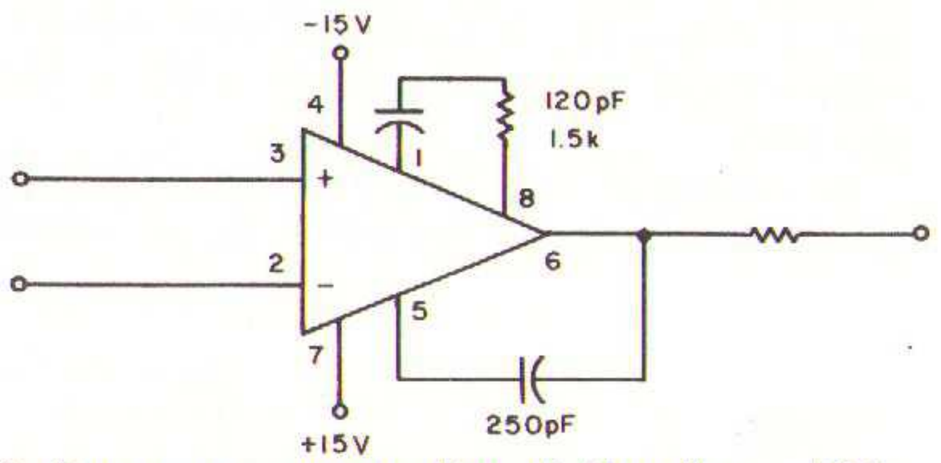
If the digital input is changed to a logical ONE, the reverse occurs and $V1_{in}$ is switched to the output.

The largest source of error in the output voltage is the offset of the op amps, which is typically 1 mV. With the compensation arrangement shown in Fig. 2, the output of the circuit is as shown in Fig. 3.

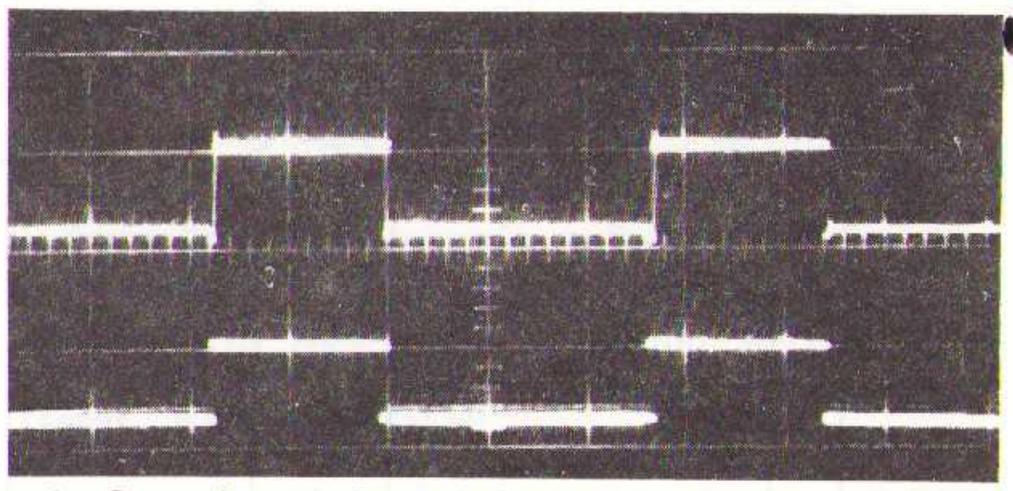
It would be possible to switch *n* voltages to the output by simply replacing the gating circuit illustrated by a *one-in-n* decoder and using *n* op amps. Negative voltages could be switched by using a pnp transistor connected to the op-amp input in place of the npn transistor in the gate, and reversing the polarity of the output diodes.



1. **When the digital input is ONE,** V_{out} equals $V1_{in}$; and when it is ZERO, V_{out} equals $V2_{in}$.



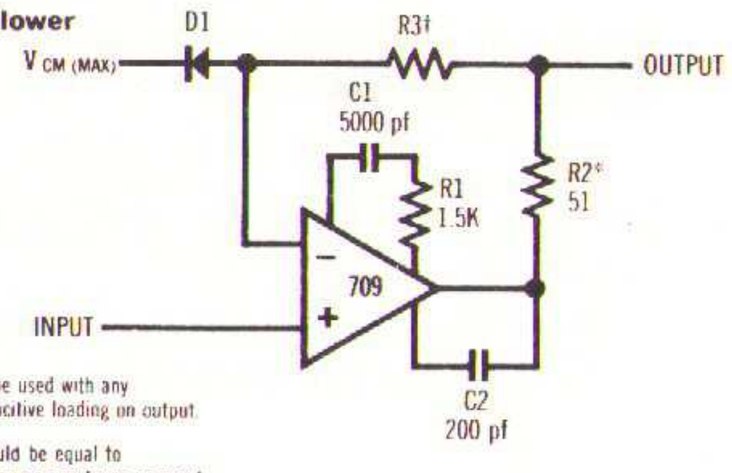
2. **Frequency compensation of Signetics 709 op amps** results in the circuit waveforms shown in Fig. 3.



3. **Operation of the switch** is shown by the output (top) and input (bottom) waveforms. Vertical scale is 5 V/div. and horizontal scale is 1 ms/div.

Typical Applications

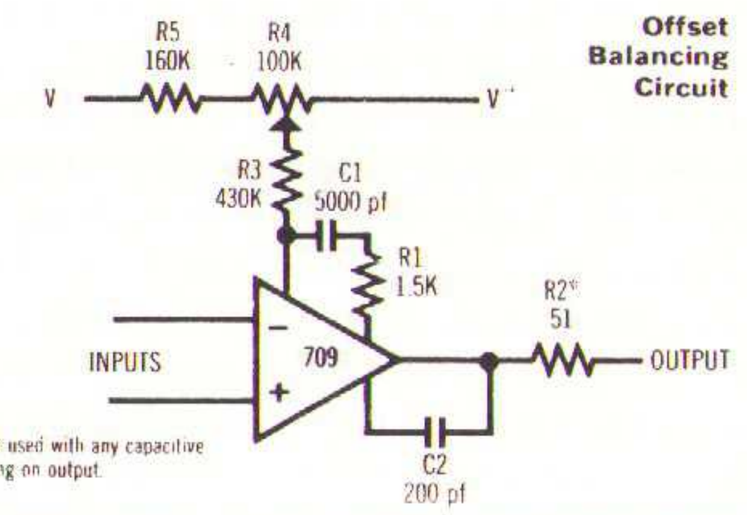
Voltage Follower



*To be used with any capacitive loading on output.

†Should be equal to dc source resistance on input.

Offset Balancing Circuit



*To be used with any capacitive loading on output.

Single op amp equalizes both amplitude and group delay

A single operational amplifier can be used as a combined amplitude and delay equalizer or as an all-pass delay equalizer. Positive or negative amplitude equalization can be achieved, resulting in either a boost or a null of a band of frequencies in the vicinity of a center frequency.

The basic circuit is shown in Fig. 1. The center frequency for the tuned circuit is:

$$F_o = 1/2\pi \sqrt{LC} \qquad (1)$$

Group delay reaches a maximum value in the vicinity of F_o and is then equal to $2RC$ (2)

The delay decreases above and below F_o.

The absolute magnitude of the gain (or loss) at F_o can be found from:

$$\left|\frac{E_{OUT}}{E_{IN}}\right|_{dB} = 20 \log_{10}\left(\frac{K-1}{2}\right) \qquad (3)$$

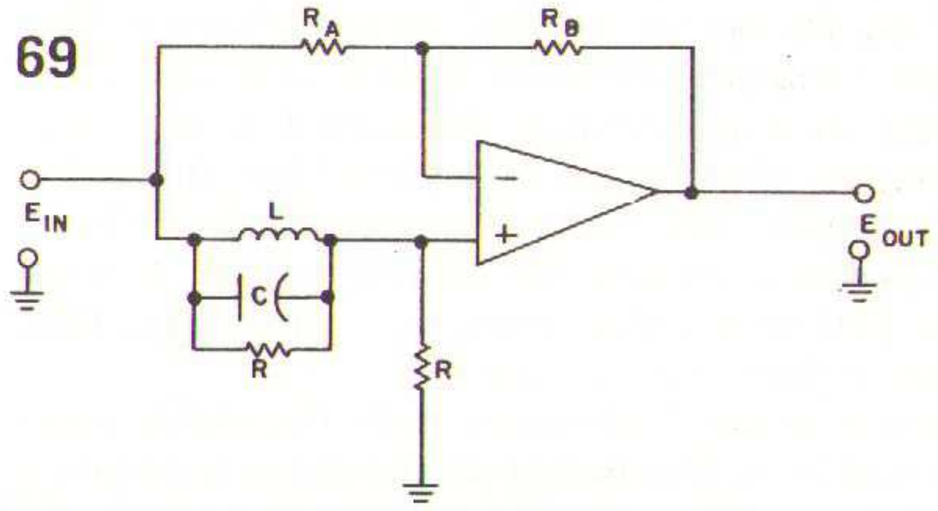
Where $K = R_b/R_a$

The actual values of R_a and R_b are not critical, except that they should be within the practical confines of the operational amplifier. The magnitude of the gain approaches unity above and below F_o for any values of K and R. The circuit will become all-pass when $K = 3$.

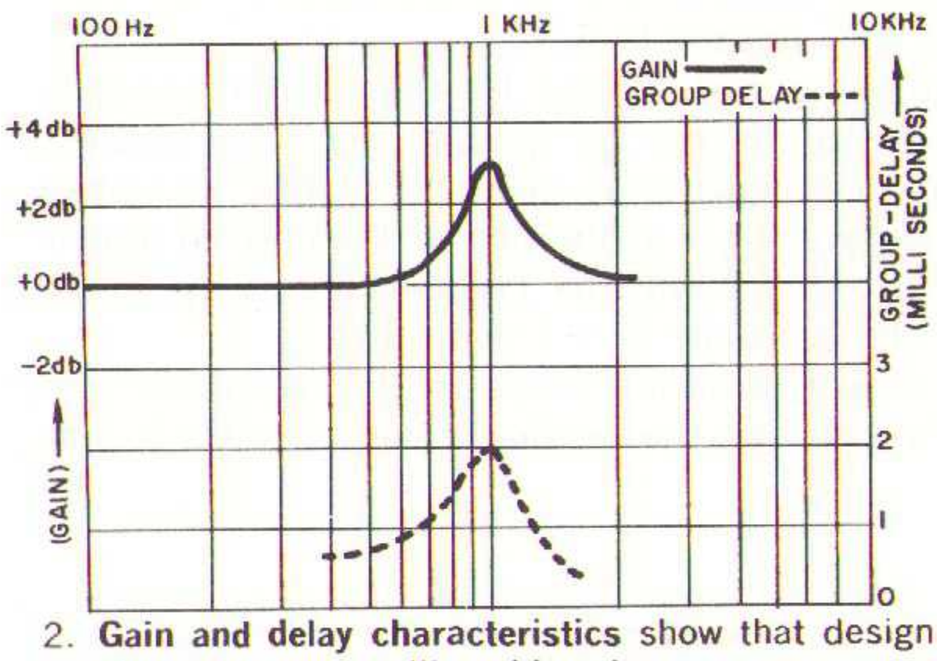
An example illustrates the complete design procedure:

Required:
2-ms delay equalization at 1 kHz
+ 3 dB amplitude equalization at 1 kHz

Procedure:
Let $C = 0.1\ \mu F$
$L = 0.253$ H (using Eq. 1)
$R = 10$ KΩ (using Eq. 2)
$K = 3.83$ (using Eq. 3)
Let $R_a = 1$ kΩ
Then $R_b = 3.83$ kΩ

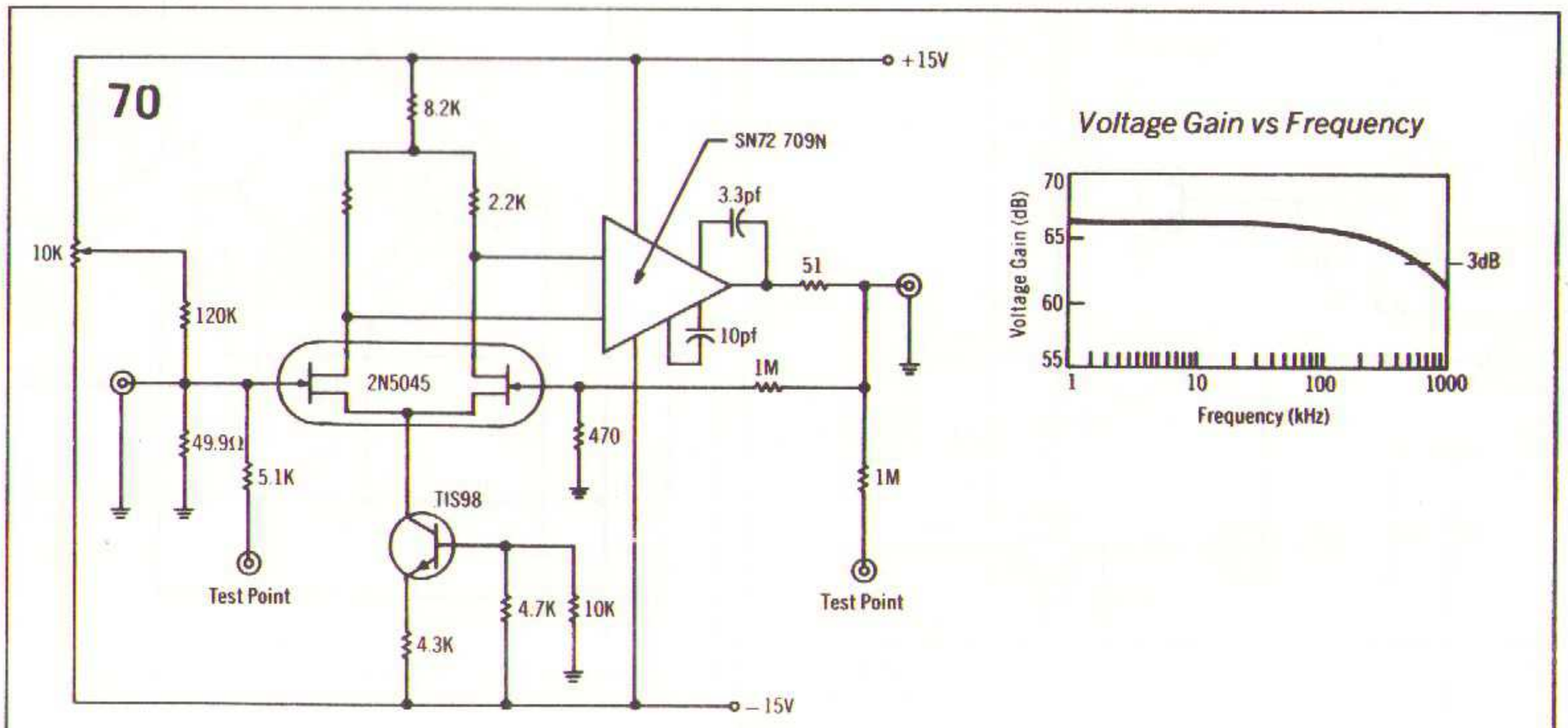


1. **Operational amplifier is combined with tuned circuit** to simultaneously equalize gain and group delay.



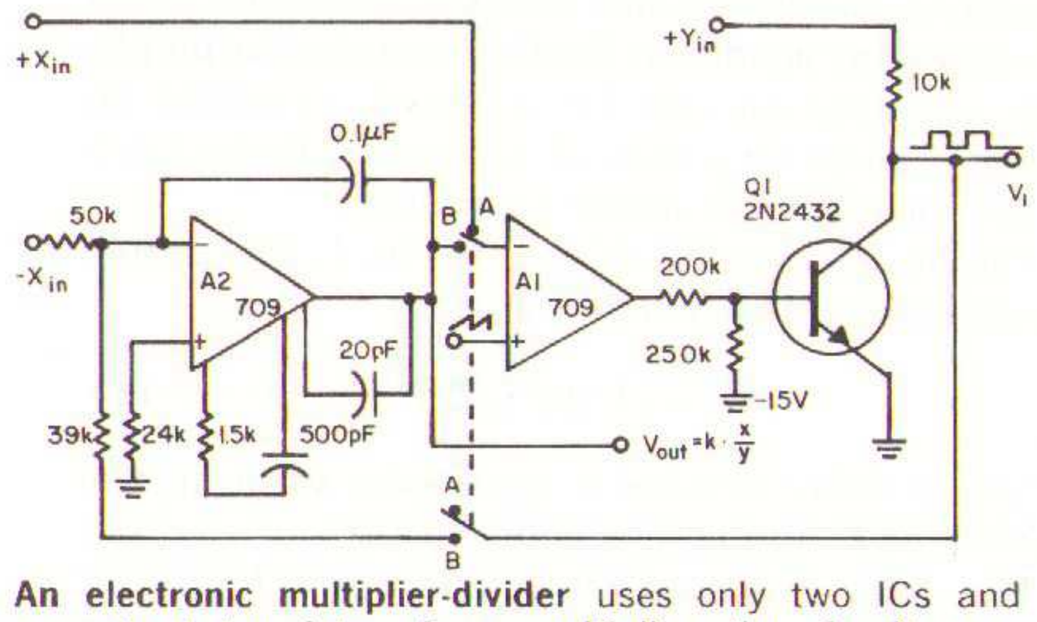
2. **Gain and delay characteristics** show that design requirements are readily achieved.

Wide-band, High-impedance Amplifier



Electronic multiplier-divider uses one or two ICs

71



An electronic multiplier-divider uses only two ICs and an output transistor. As a multiplier, the circuit uses only A_1 and the output transistor. A divider results when the second stage and the feedback loop are connected.

In simulation work with analog computers one frequently needs a simple multiplier or divider. Here is a circuit that performs the functions of both, and can be built quickly in any reasonably equipped laboratory (see schematic). Its only requirement is that the variables to be multiplied or divided are either $+x$, $+y$ for the multiplier, and $-x$, $+y$ for the divider.

When the circuit is used as a multiplier, the switch bypasses the first stage. The amplifier A_1 acts as a comparator. Its output is negative as long as the x-input is higher than the sawtooth voltage. When the linear sawtooth voltage exceeds the x voltage, the polarity of the A_1 output is reversed and Q_1 goes into saturation. The output voltage goes to zero.

Thus a pulse is obtained with the width proportional to x. The height of the pulse is proportional to y. The average dc output voltage is given by $V_{1(avg)} = kxy$.

Because of the op amp type used, the sawtooth voltage is limited to 5 V. Consequently the x-input is also limited to 5 V.

The y-input is limited by the collector-to-base breakdown voltage of Q_1 (30 V). The highest sawtooth frequency is about 10 kHz. The upper frequency limit is a function of the desired multiplier accuracy. For the frequencies of up to 10 kHz, the accuracy is ± 1 per cent.

Adding the second stage to the multiplier circuit and closing the feedback loop converts it into a divider. It has a very high gain. Now the average voltage obtained at the collector of Q_1 is proportional to the voltage at the inverting input of op amp A_2. Remembering our previous multiplier description, we can write:

$$V_1 = kV_{out}y.$$

But since $V_1 = x$, we can directly obtain

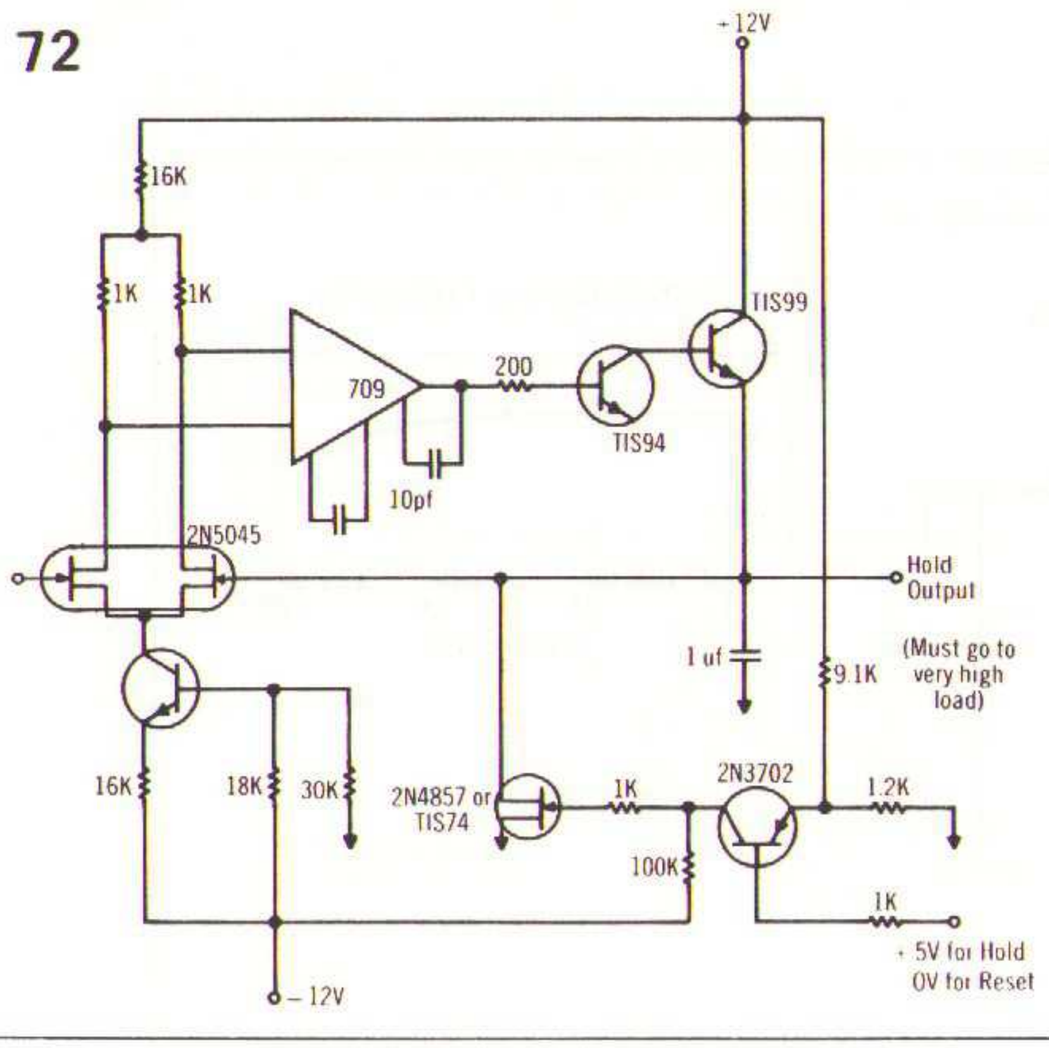
$$V_{out} = kx/y,$$

which simply says that now the output voltage is proportional to x divided by y.

The highest sawtooth frequency here is again 10 kHz. The frequencies of x and y should not exceed 100 Hz, since the loop gain decreases with the increasing frequency. This lowers the accuracy of the divider. Furthermore, to prevent saturation, one must always have $|x| < y$.

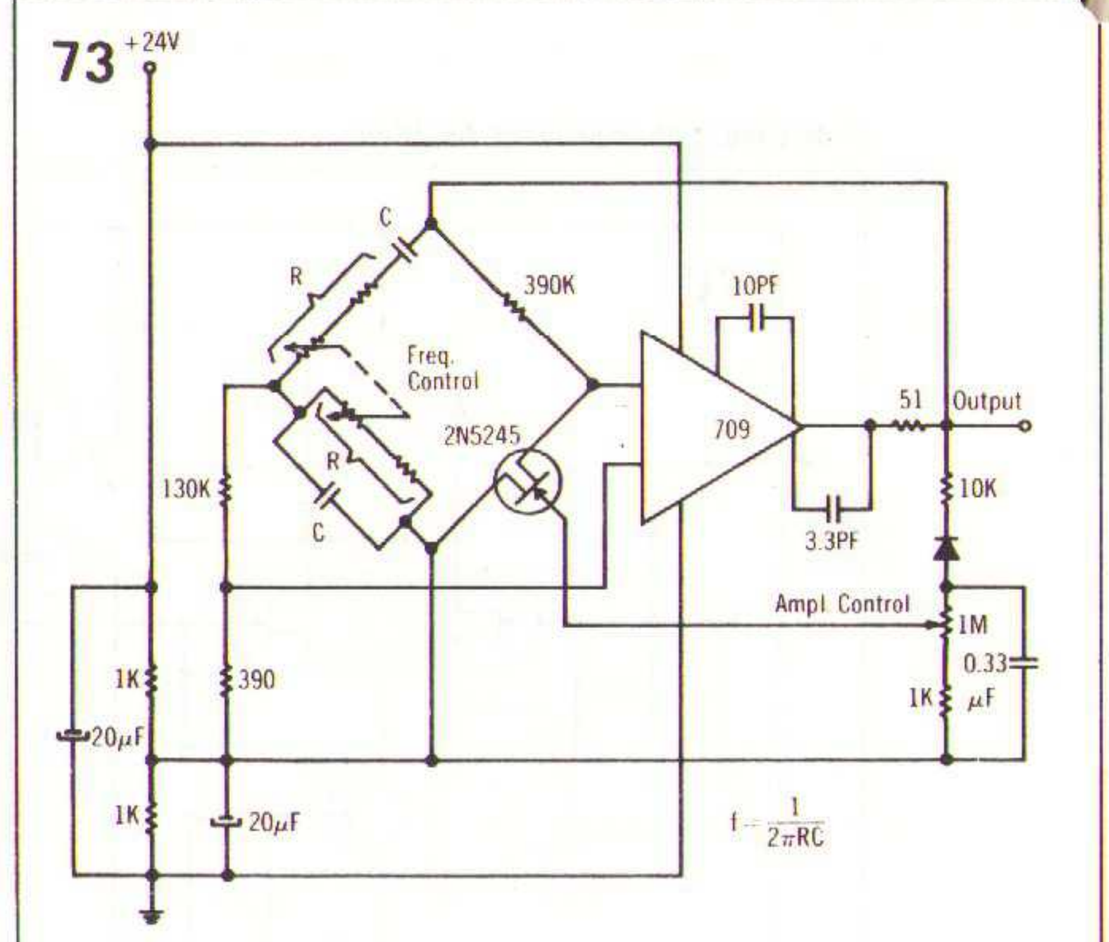
Peak Detector

72



Wien-Bridge Oscillator

73



Convertisseur tension-courant

Nomenclature:

C1, C2: 0,1µF 60V
C3 : 4,7nF 60V
C4 : 220pF 60V
C5 : 1 nF 60V

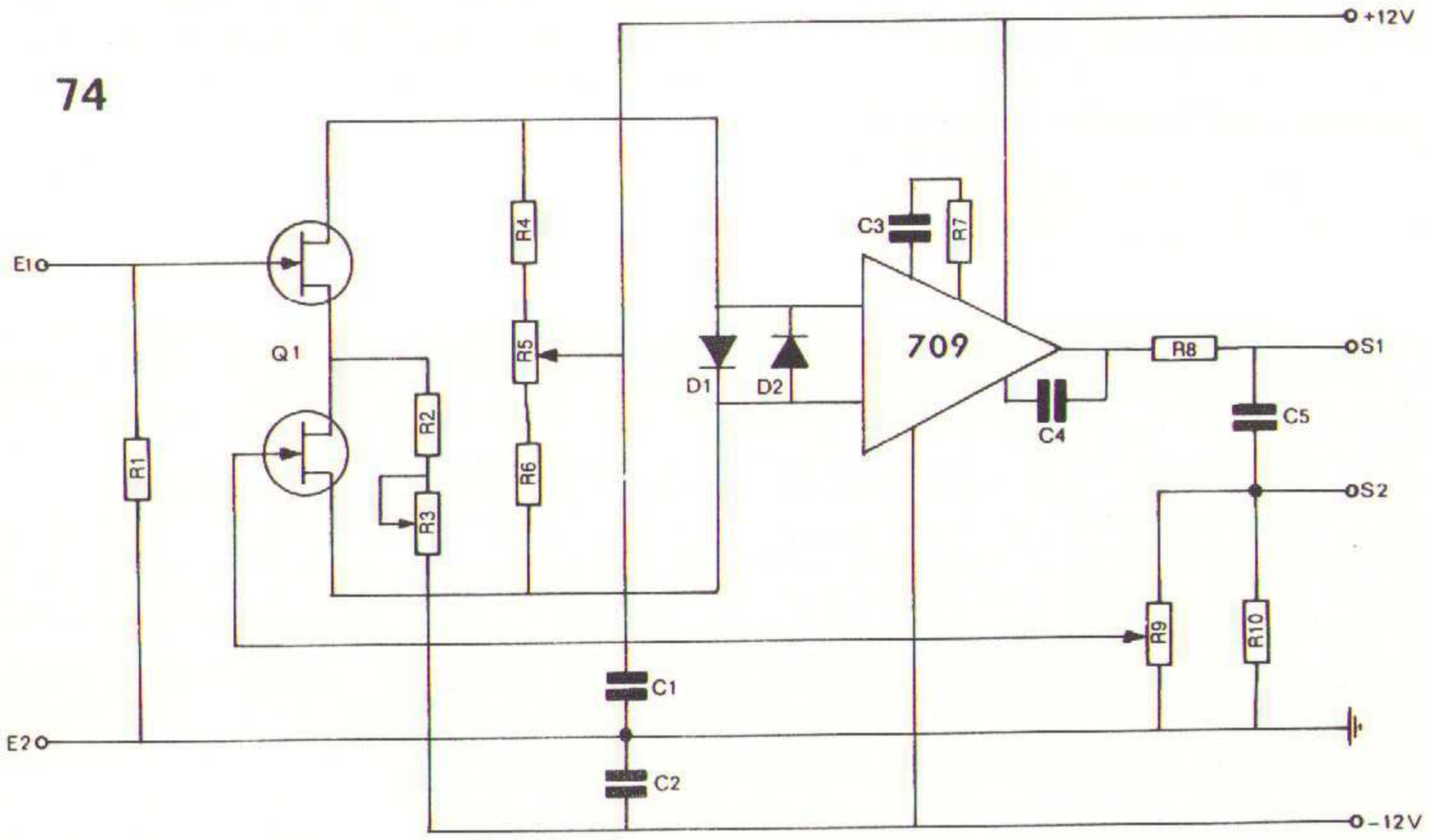
Q1 : TIS 68

D1, D2: 1N4148

R1: Suivant impédance d'entrée désirée: 100kΩ ou 1MΩ.
R2: 12kΩ 2% KΘ: 25.10-6
R3: 5 kΩ Bobiné
R4: 12kΩ 2% KΘ: 25.10-6
R5: 2 kΩ Bobiné
R6: 12kΩ 2% KΘ: 25.10-6
R7: 1,5kΩ 5%
R8: 100Ω 5%
R9: 5 kΩ Bobiné
R10: 250Ω 1% KΘ: 25.10-6

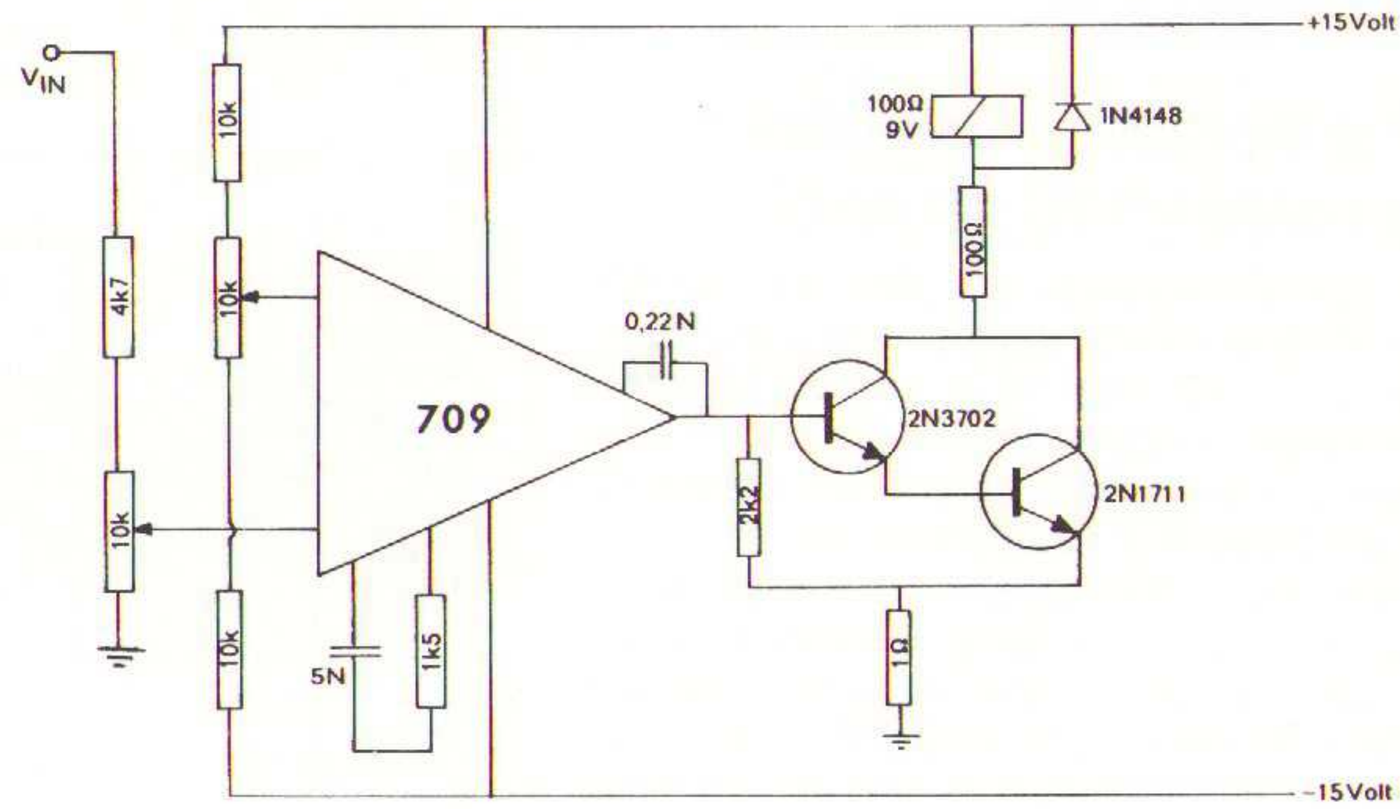
Amplifier: SN 52709 ou SN72709.

74



Differential switch

75



Narrow-band rejection filter uses twin-T

In the course of low-frequency amplifier design, it is often necessary to have a narrow-band rejection filter. At vlf, inductors are excessively large, and this suggests the use of an RC filter. The twin-T has theoretically infinite rejection at its null frequency; however, it is unsuitable for narrow-band work since its bandwidth is four times its center frequency. Since the RC passive filter doesn't meet the specifications, the use of an active filter is indicated.

By placing the twin-T in the forward loop there is no transmission at the null frequency.

If the twin-T has a transfer function of

$$H(s) = (s^2 + \omega_o^2)/(s^2 + B_w s + \omega_o^2)$$

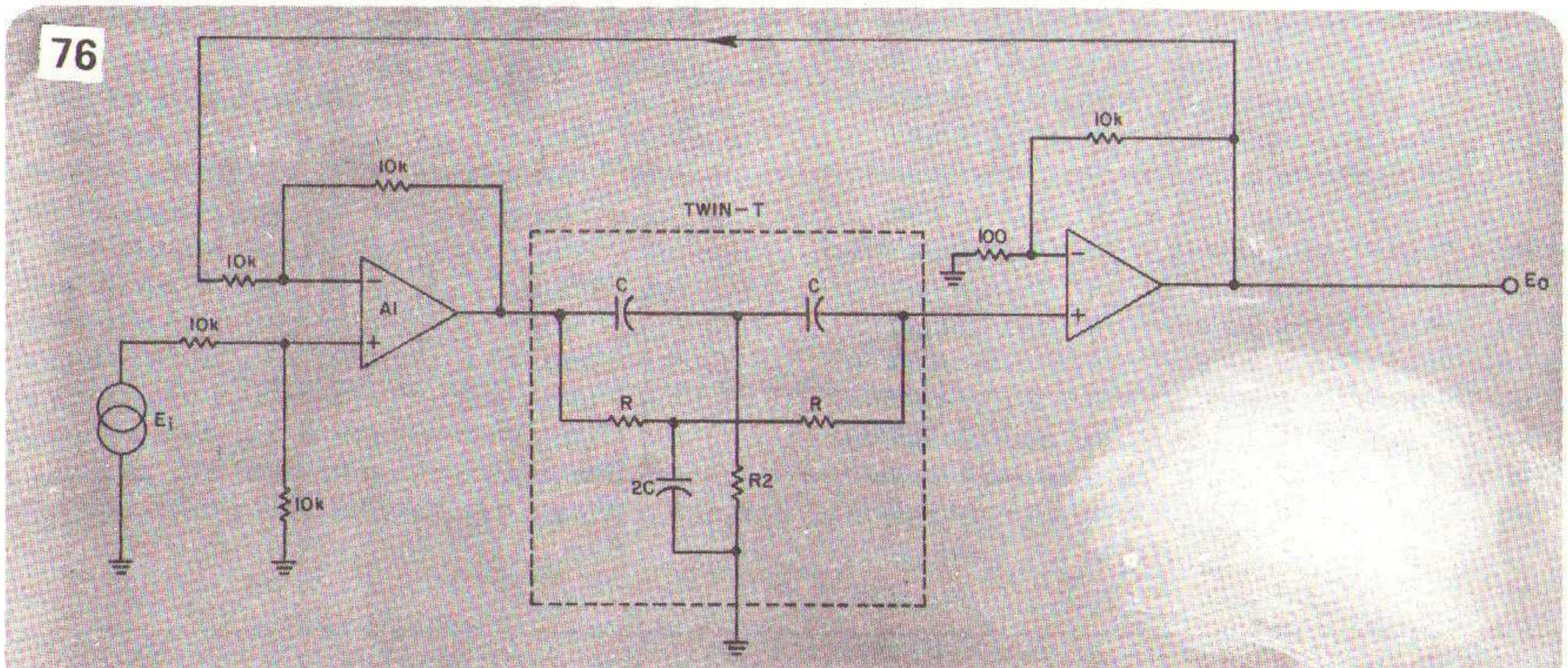
the over-all system has a transfer function of

$$\frac{E_o(s)}{E_i(s)} = \frac{k}{k+1} \cdot \frac{s^2 + \omega_o^2}{s^2 + \frac{B_w s}{k+1} + \omega_o^2}$$

where k = amplifier gain, ω_o = filter center frequency in radians and B_w = filter bandwidth of $H(s)$. It can be seen that the passive network bandwidth has been narrowed by the factor $k + 1$.

The circuit uses two IC amplifiers. Amplifier 1 is simply a subtractor, and amplifier 2 supplies gain with no inversion. This circuit at its null frequency has rejection greater than 40 dB and bandwidth of 0.04 ω_o with a gain of 100 in A2.

The circuit has the advantage of driving the twin-T from a low impedance and terminating it in a high impedance.



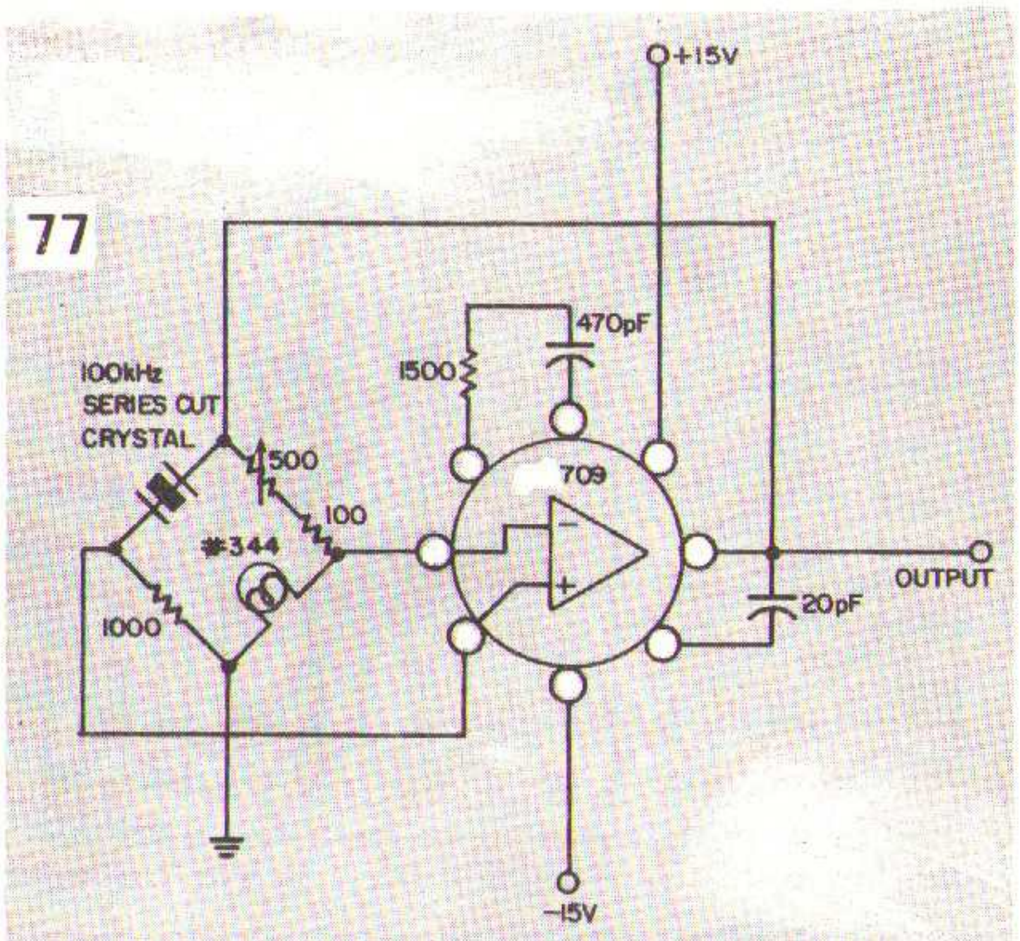
Narrow-band amplifier using twin-T requires two operational amplifiers.

Transformer-less Meacham bridge employs IC op amp

An untuned version of the well-known Meacham Bridge crystal oscillator can easily be built with an IC op amp (Fig. 1). Unlike many other IC crystal "clocks," this one maintains the crystal drive at a constant level, thus improving the circuit's frequency stability.

A #344 lamp on the negative feedback side of the bridge acts as a nonlinear element (Fig. 2) to cause an increase in the negative feedback factor when the output increases. This operating point stabilization is similar to that used in most RC audio generators.

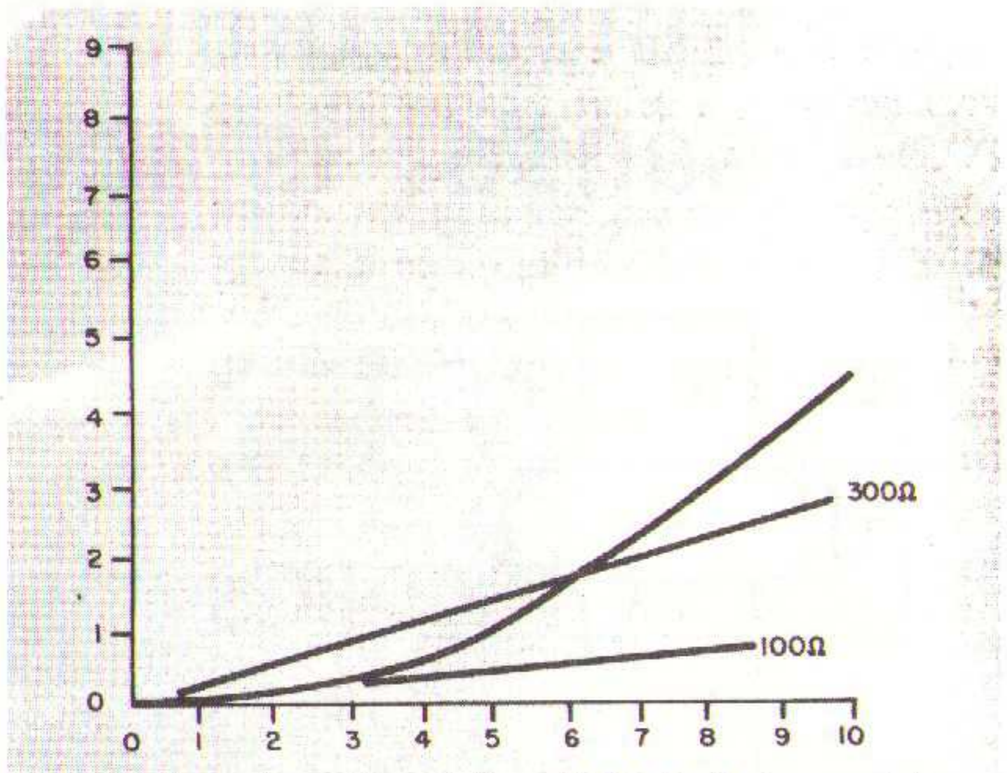
Since the lamp operates at about 100 Ω and the



1. **No transformer** is used in this Meacham Bridge. An IC op amp is combined with a light bulb to keep the crystal drive level fixed.

crystal series resistance at series-resonance is about 1000 Ω, it is not possible to make all of the bridge arms equal. This would improve the stability of the design.

By using a vacuum-mounted crystal, with a lower series resistance, the all-equal-arm aim could be approached. Also, as op amps with higher frequency cutoffs become available, AT-cut crystals above 1 MHz could be used in similar designs. These crystals have about 100 Ω of series resistance near 2.5 MHz and would seem to be naturals for such a Meacham Bridge.



2. **The nonlinearity of the #344 bulb** is used to increase the negative feedback factor when the output increases. 100 Ω and 300 Ω lines are shown for reference.

IC ramp generator is simple and fast

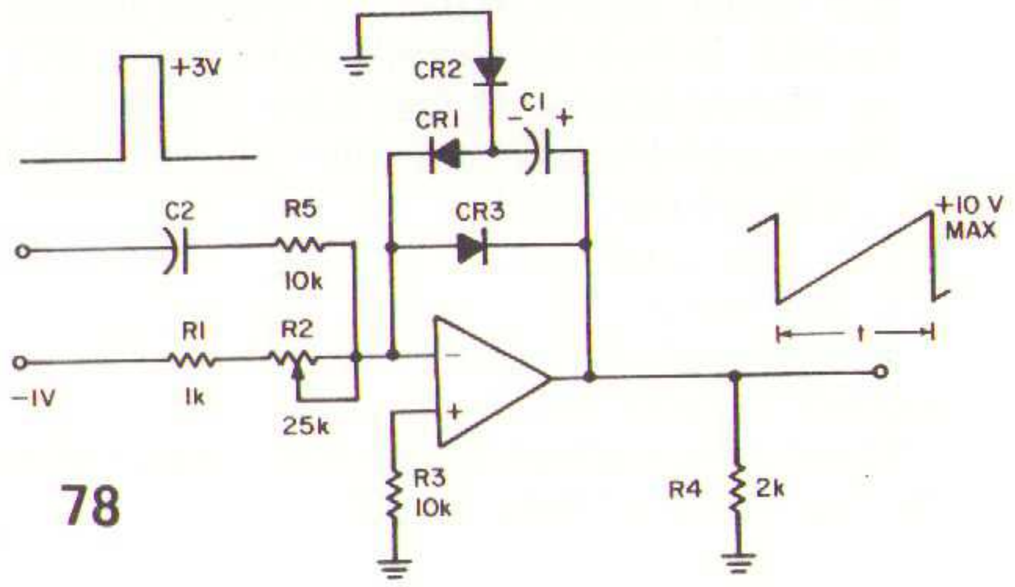
One of the more familiar uses for an operational amplifier is as an integrator. Since the output voltage lamp for most available op-amps connected as an integrator is fairly linear, it would seem logical to develop these linear ramp functions into sawtooth generators. This mode of operation requires a circuit that has an output with a definable and adjustable rate of rise and an instantaneous, or at least an extremely fast, fall-time characteristic.

Such a circuit is shown in the figure, and its operation is as follows.

With a small amount of offset voltage connected to the (—) input of the operational amplifier, the output will rise in the positive direction at a rate governed by the time constant of C, R_1 and R_2.

The polarity of the current flow to charge C is such that the diode CR_1 will conduct. The capacitor, effectively connected to the input, then completes the feedback loop.

A positive pulse applied to the input through R_5 overcomes the negative offset voltage and the output tends to fall in the negative direction. This reverses the current flow to disconnect the feedback capacitor from the circuit by back-biasing CR_1. CR_2 discharges the capacitor, thereby preventing the circuit from remembering its

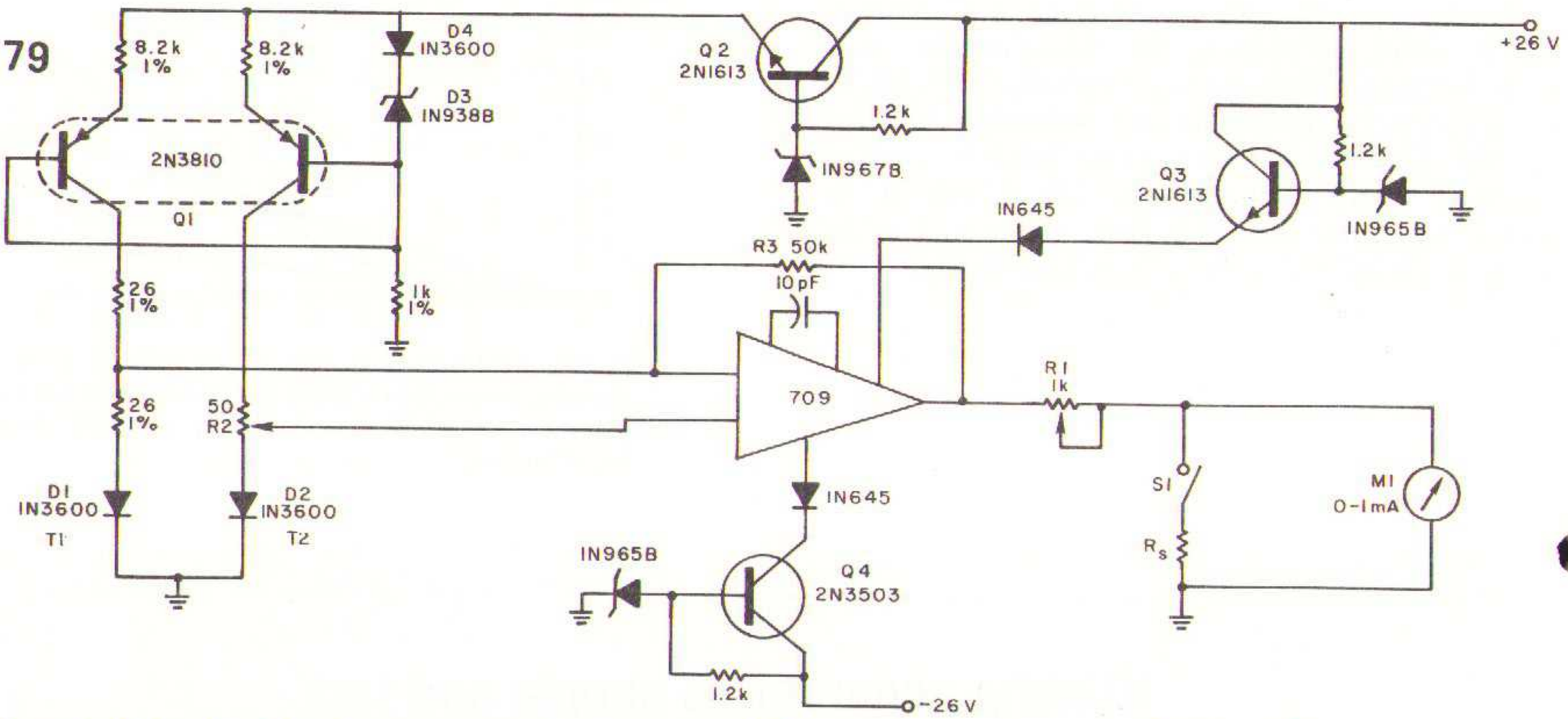


Ramp generator has a fast fall time and is fairly linear. All diodes can be any germanium types. The value of C is selected to provide the desired period.

last output level. CR_3 clamps the output to zero by reducing the feedback path to a short and preventing negative saturation.

When the positive pulse is removed, the negative offset voltage is again integrated, and the output begins to rise towards the positive saturation point until the next positive pulse resets it again.

Linear differential temperature sensor is accurate and simple



Linear differential temperature is measured with this circuit. Temperatures are sensed with D_1 and D_2.

Frequently a linear differential temperature measurement independent of room ambient is desired. It can be made easily by sensing the voltage drops across a pair of silicon diodes (see figure). Before we describe the circuit, let's give the theory behind its operation.

The current-voltage relation of small signal diodes is approximately

$I = I_s\,[\exp(qV/\eta KT) - 1]$.

Rearranging,

$V = \ln\,[(I + I_s)/I_s]\;T/(q/\eta K) = CT$,

where C = constant.

Given two identical diodes with equal currents flowing through them, we get

$V_1 = CT_1$,

$V_2 = CT_2$,

where T_1 and T_2 are temperatures experienced by diodes 1 and 2, respectively.

The voltage differential under these conditions is

$V = (V_2 - V_1) = C(T_2 - T_1)$

and is a linear function of the diode temperature difference.

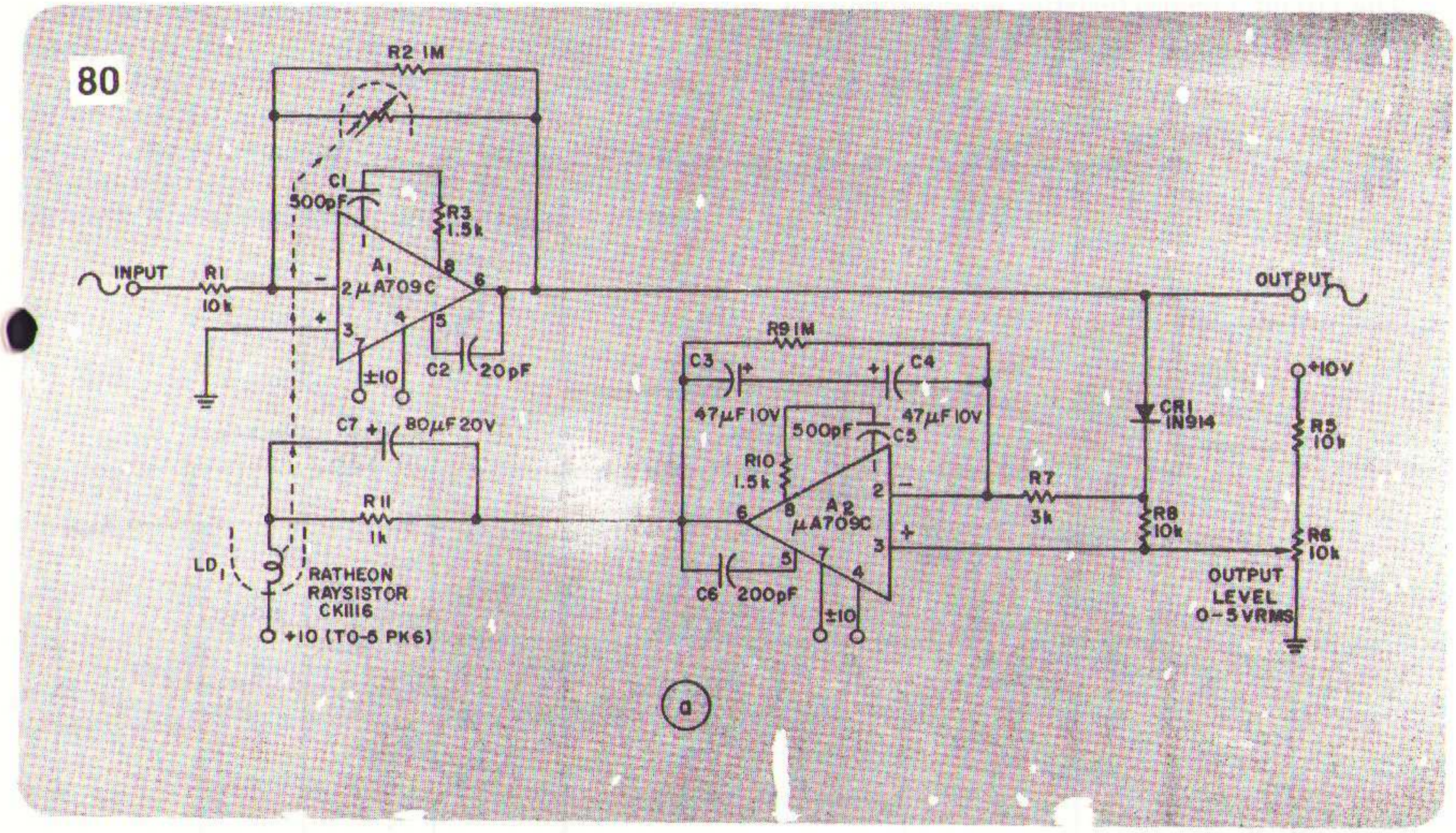
The figure shows the straightforward design providing full-scale readout of either 1 or 10 differential deg F. The circuit is built with standard parts and is easy to construct. Q_2 through Q_4 provide regulated voltages. Q_1 is a dual transistor and provides identical currents to sensor diodes D_1 and D_2. Calibrated operation over wide ambient temperature ranges is obtained with a zero temperature coefficient zener diode D_3. In series with the zener diode is a silicon diode D_4, which matches the temperature coefficient of the base-emitter diode of Q_1.

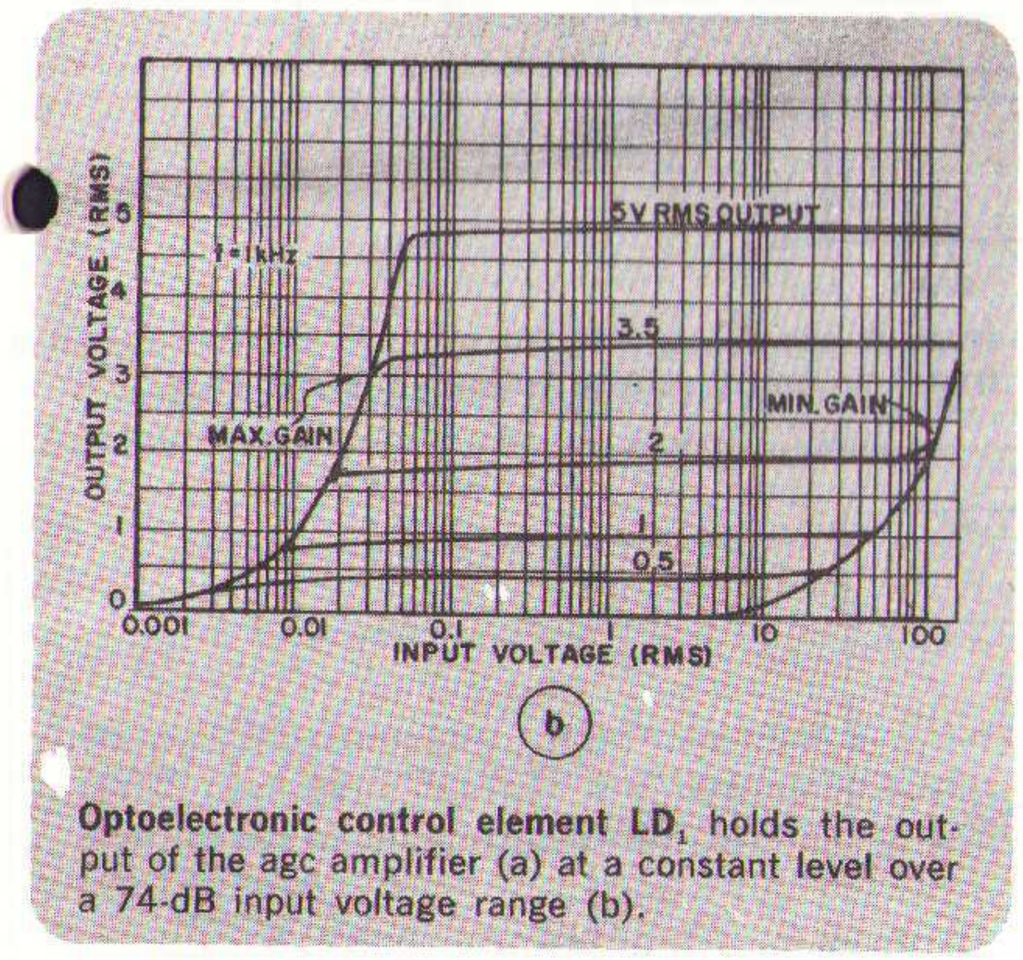
Potentiometer R_2 allows nulling of the system. Feedback resistor R_3 sets the op amp gain. The scale factor for meter M_1 is set by R_1. For the correct setting of R_1, the meter full scale deflection corresponds to 1°F. Switch S_1 connects a shunt (R_s) across the meter for the full scale deflection of 10°F.

Wide-range agc amplifier uses optoelectronic control circuit

Optoelectronic components have zero signal distortion and extremely wide dynamic range. Therefore an audio agc amplifier that uses an optoelectronic device as the control element will have excellent characteristics.

In the circuit (a), LD_1 consists of a lamp and photoresistor in a TO-5 package. If the output voltage exceeds the reference set by R_{11}, an error voltage is generated by amplifier *A2*. This error voltage increases the power to the lamp of LD_1,





Optoelectronic control element LD_1 holds the output of the agc amplifier (a) at a constant level over a 74-dB input voltage range (b).

thus lowering the resistance of the photoresistor, which in turn decreases the gain of *A1*. A constant output level results.

R_{11} and C_7 form a compensating network, which improves the transient characteristics of the control system by canceling a pole in the transfer function of LD_1.

Frequency of the circuit is flat from 5 Hz to 220 kHz at 1-V rms input and output.

Complementary audio amplifier has low distortion, high output

An integrated-circuit operational amplifier, connected as shown in the figure, makes an excellent class AB audio amplifier for driving either headphones or speakers.

This circuit is a stabilized dc amplifier. It has low distortion, high power gain, low idling current and wideband operation. It can deliver a power output of 8 W into a 4-ohm headphone, and it can operate from any supply voltage between +6 to +15 V.

The circuit's characteristics are as follows:

Power output	= 2.0 W @	R_L = 16 ohms.
	4.0 W	R_L = 8 ohms.
	8.0 W	R_L = 4 ohms.
Input impedance	= 10 k.	
Frequency response	= 5 Hz to 50 Hz ±1 dB.	
Harmonic distortion	= less than 0.3 per cent at full power at 20 Hz to 20 kHz.	
Gain	= 11.	

An input signal of 0.5 V is required to deliver full power into a 4-ohm load.

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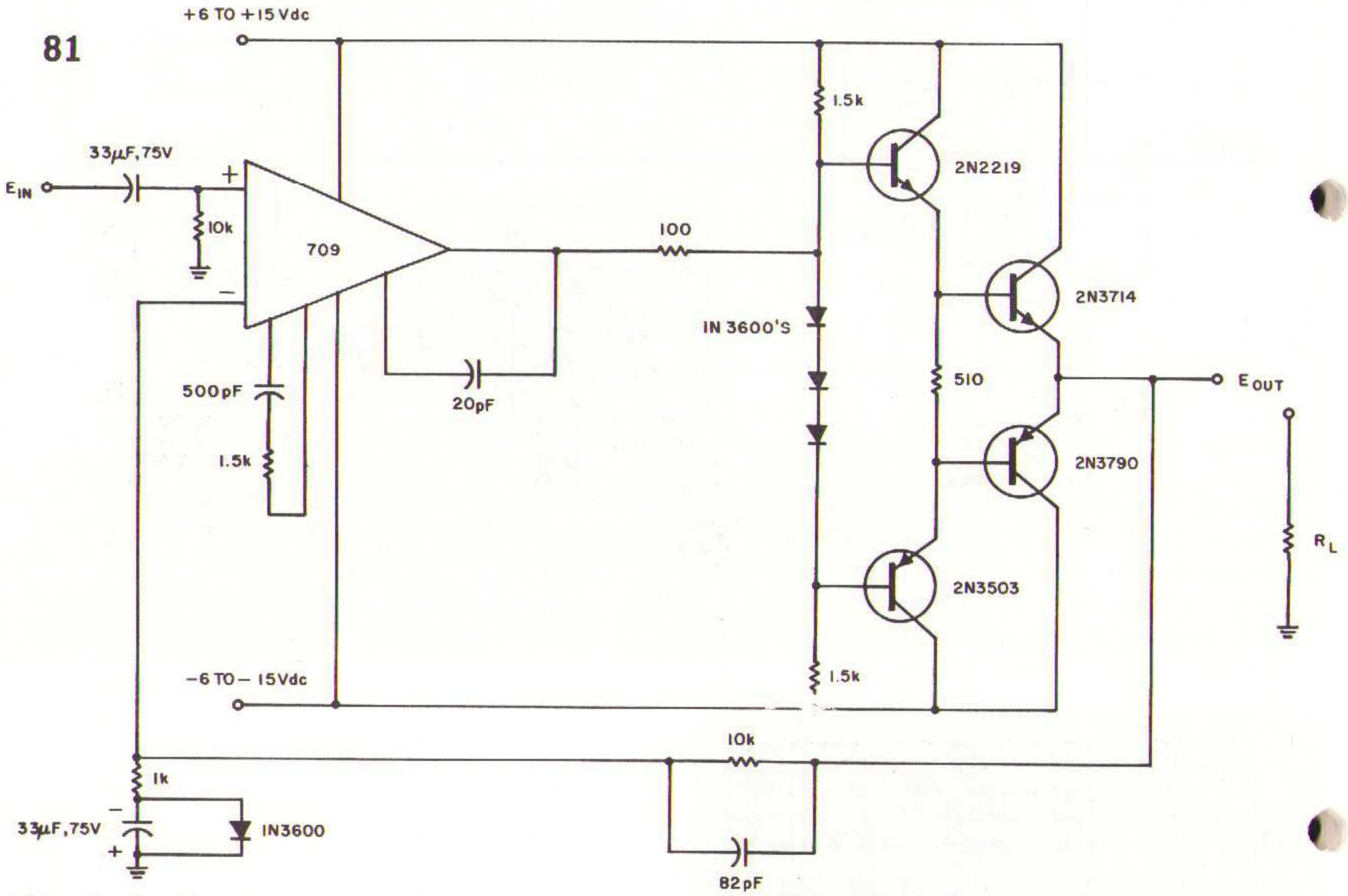
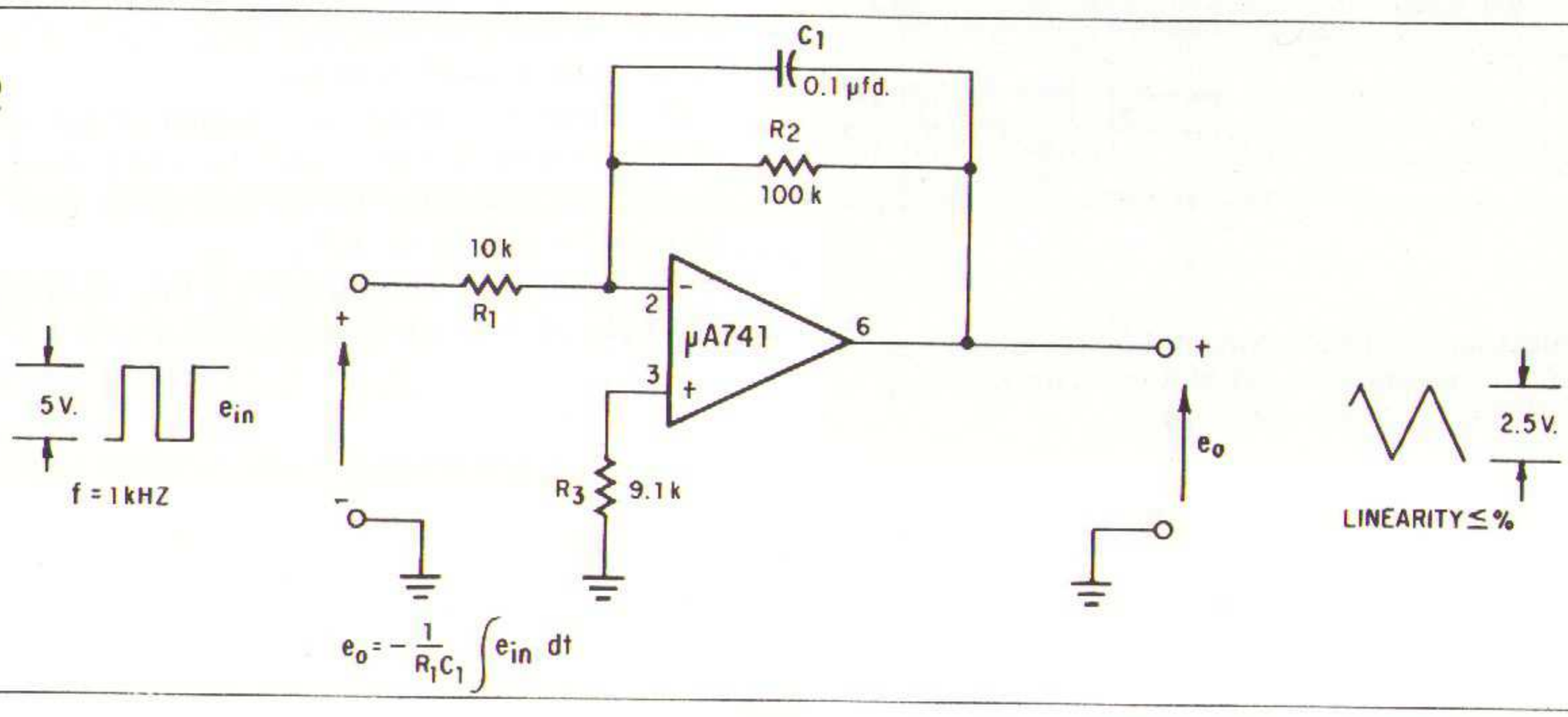


High-gain, low-distortion audio amplifier results when an op amp is combined with a complementary power output stage. It can deliver 8 W into a 4-ohm speaker, operating from any supply voltage between +6 and 15 V.

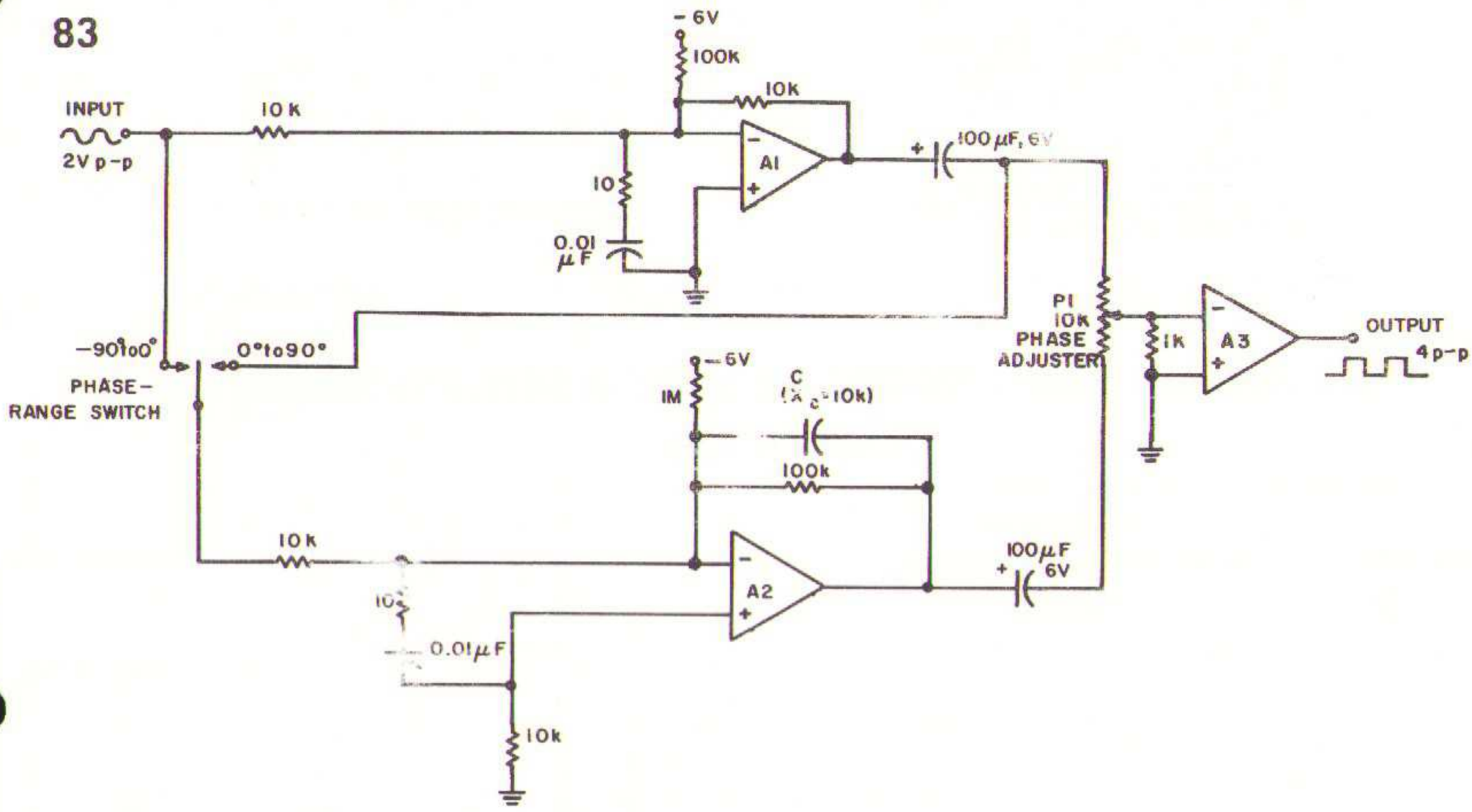
82



Generate variable-phase square waves this cheap, easy way

Converting a sine wave into a constant-amplitude square wave with adjustable phase shift is often necessary in such circuits as phase-sensitive detectors. A very satisfactory solution to this need, using inexpensive monolithic operational amplifiers and operating over the full 0° to 180° range, is shown in the figure.

Amplifier *A1* is an inverting sine wave generator, and *A2* is a cosine generator. The outputs are summed together by *A3* with relative weighting controlled by *P1*. The input to *A3* is thus a sinusoid whose amplitude and phase are determined by the amplitudes of the input sine and cosine waves. Because *A3* is operated open-loop, it acts as a zero-crossing detector generating a constant amplitude square wave whose phase can be adjusted from −90° to +90°. The circuit can be used at any frequency from 10 Hz to 1 MHz by setting the reactance of C to 10 kΩ at the desired frequency.



Operate at any frequency from 10 Hz to 1 MHz by simply choosing X_c to be 10 k-ohms. Amplifiers A1 and A2 are type 709 ; A3 is a type 710 Potentiometer P1 controls the phase.

Circuit converts two analog quantities to frequency or period

Circuits that produce output signals with a frequency or period proportional to one or more analog quantities find widespread use in control and measurement systems.

One such circuit for converting two analog quantities, X and Y, into an output signal that has a frequency $f = kY/X$ or a period $T = kX/Y$ is shown in simplified form in Fig. 1. The circuit inputs, derived from the analog quantities, are current I and voltage V.

In operation, the input current I charges capacitor C through resistor R_1. When the potential of point M reaches that of point N, the amplifier output, initially at some positive voltage $+E_1$, switches to a negative voltage $-E_2$. This forward biases diode D and switches transistor Q on.

As a result, point N abruptly drops very close to ground potential, and C discharges through the forward biased diode. When the discharge of C again brings point M to the same potential as N, the amplifier output switches back to $+E_1$. This reverse biases D and turns Q off, so the circuit is prepared for the next cycle. The amplifier, therefore functions as a dual-level voltage comparator. A necessary condition for operation of the circuit is that the discharge time for C be very short compared to the charging time.

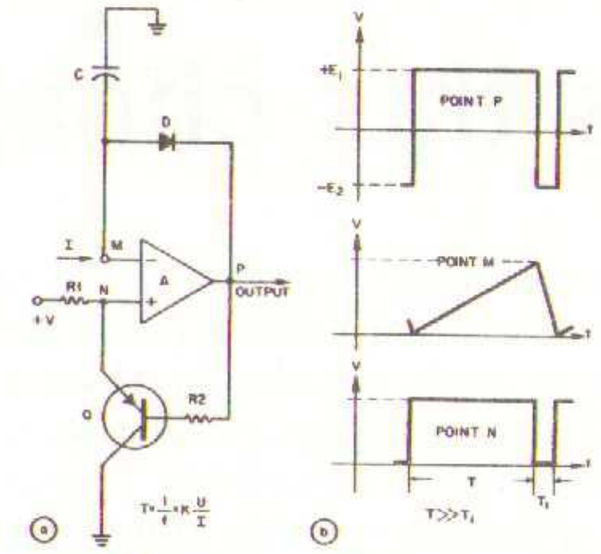
It is clear from the preceding description that the duration of one cycle is proportional to the voltage V and inversely proportional to the current I, or

$T = 1/f = k(V/I)$.

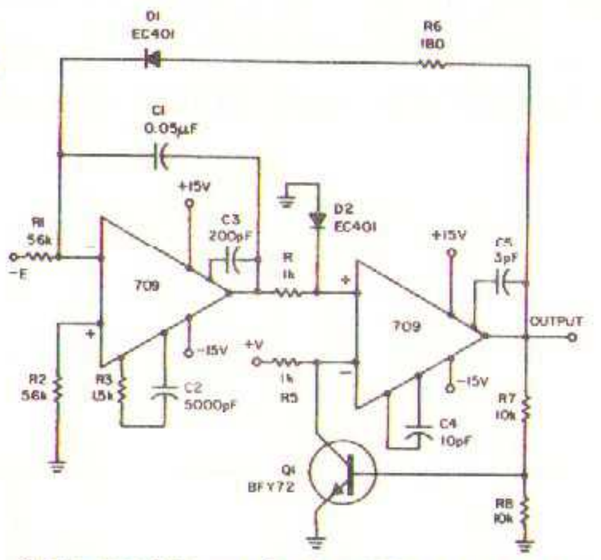
So the circuit converts either V/I to period or I/V to frequency. If the current I is held constant, then $T = kV$. Similarly if V is constant, $f = kI$.

Under the condition $T >> T_1$ (Fig. 1b), conversion error in the circuit arises only from the finite value of V_{CE} for the switching transistor. Likewise, conversion stability depends only on the stability of the V_{CE} value. If a transistor is used that has a V_{CE} less than 10 mV and good high temperature stability, the conversion error of the circuit can be less than 0.1%.

A complete circuit of this type, suitable for practical applications, is shown in Fig. 2. Measurements have shown it to be stable, accurate and linear, with errors on the order of 0.1% for input quantity variations of more than 40 dB.



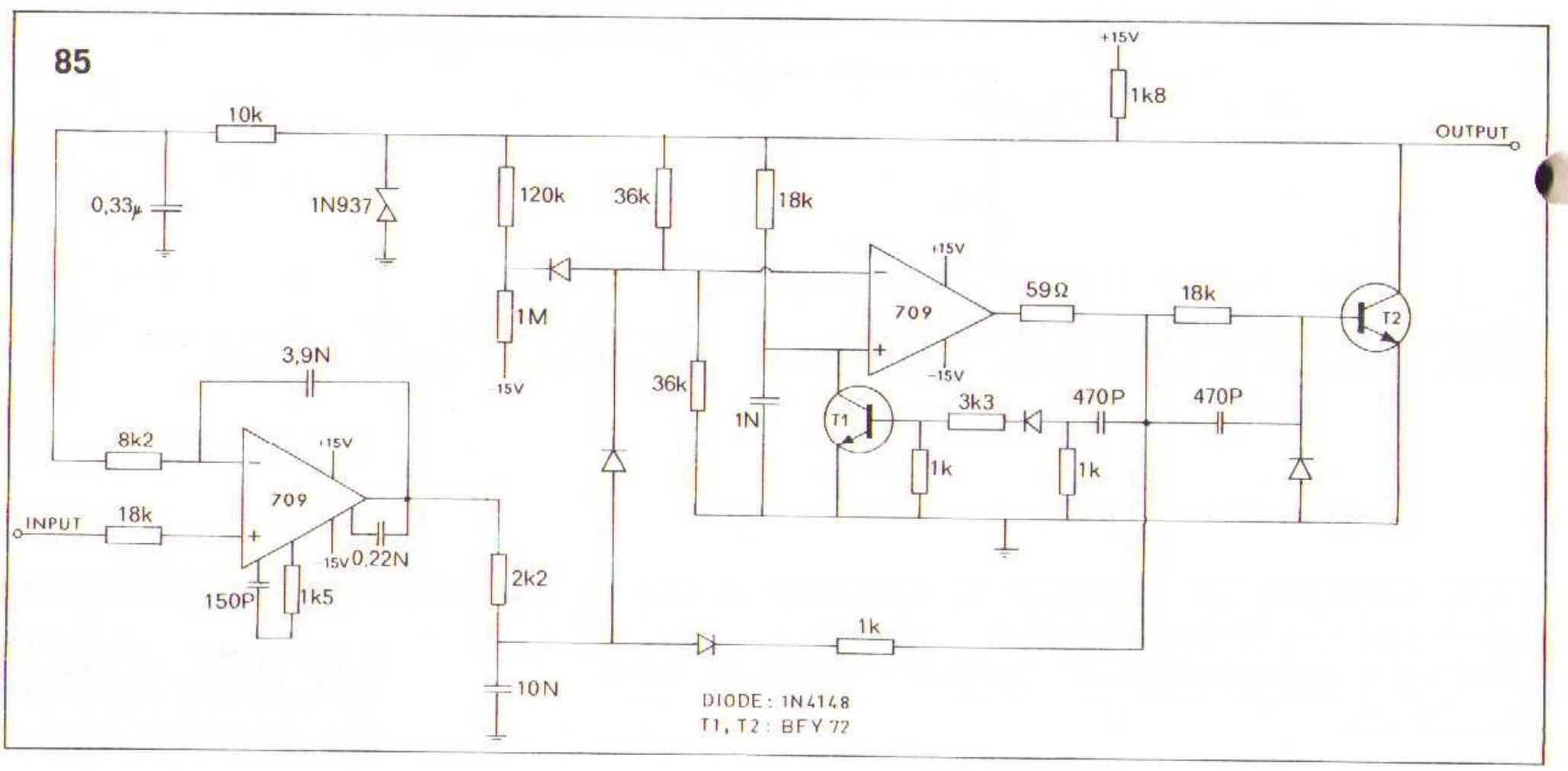
1. **Amplifier A functions as a dual-level comparator** (a). It compares the voltages at points M and N, and switches the output level at P each time they are equal (b).



2. **Two monolithic operational amplifiers** are used in a practical version of the converter.

A/D CONVERTER CIRCUIT CONVERTS ONE ANALOG QUANTITIE TO FREQUENCY.

(lin.: ≤ 0,01%)



HIGH QUALITY VOLTAGE CONTROLLED GAIN BLOCK

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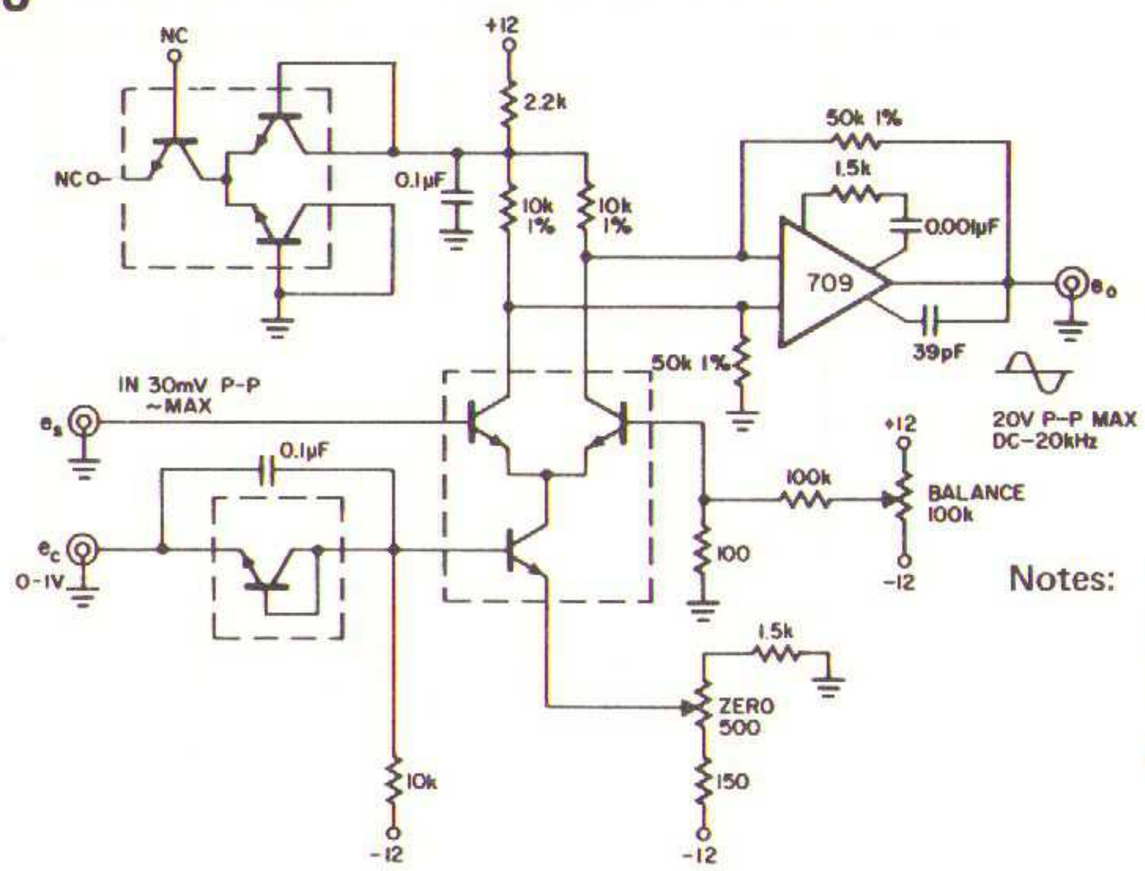
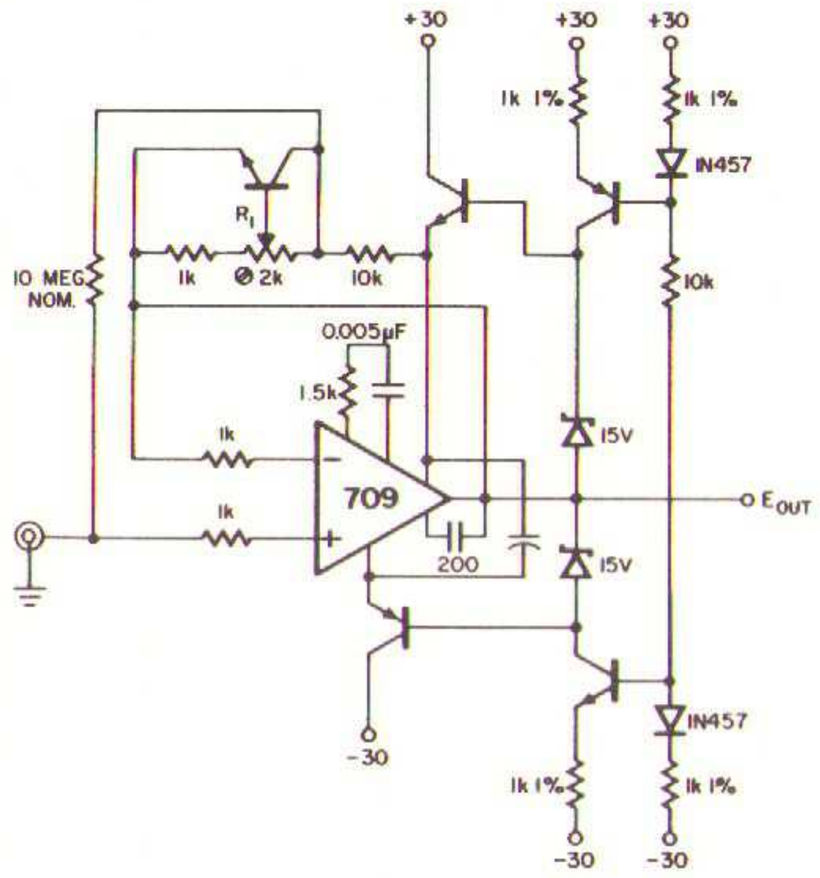


Notes:
1. Adjust zero for 20dB of gain at $e_c = 0$.
2. Adjust balance for $e_o = 0$ vdc at $e_c = 1V$.
3. $e_o/e_s \cong 10 + 1000\ e_c$ for $o \leqslant e_c \leqslant 1V$.
4. Noise and distortion $\leqslant 0.5\%$ for all settings of e_c. $e_s = 20mV$ p-p, 20Hz – 20kHz.

HIGH VOLTAGE 1000 MEGOHM DC AMPLIFIER

87



Notes:
1. $R_{in} > 1000$ megohms for $-10V \leqslant E_{in} \leqslant +10V$.
2. Bias current adjustable to zero by means of R_1.
3. Tracking error $< \pm 0.1mV$ for $-10V \leqslant E_{in} \leqslant +10V$.
4. Transistors are low leakage, $V_{ce_o} \geqslant 60V$, $hf_e \geqslant 50$. (2N2102/2N4036 or equivalent)

A A N T E K E N I N G E N N O T E S

Andere toepassingen van de 709 operationele versterker treft U aan in:

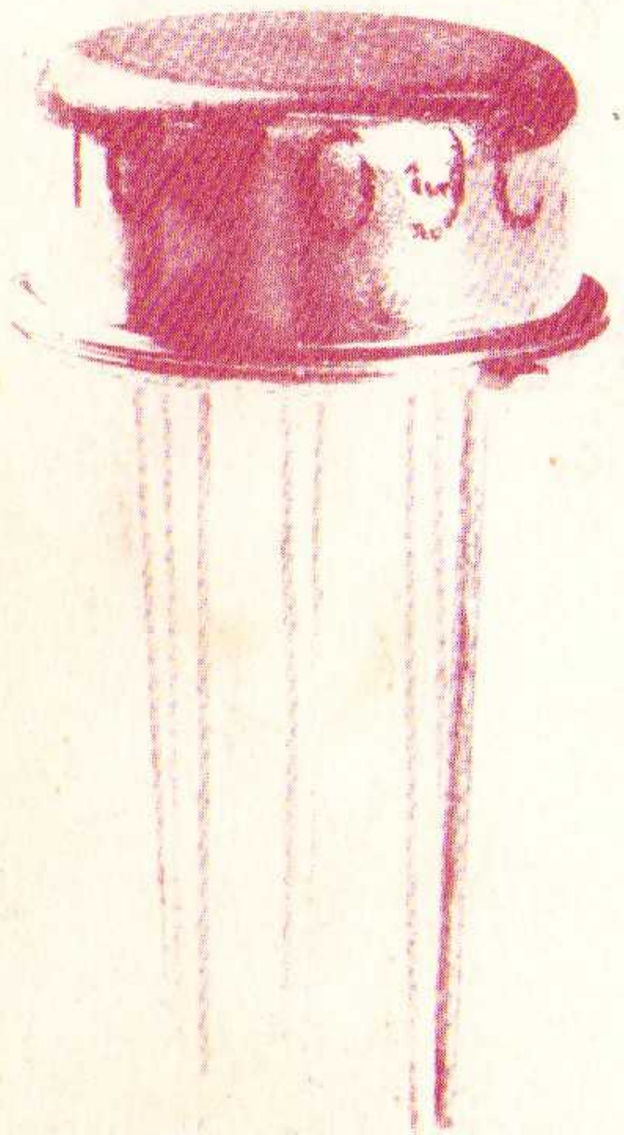
schakeling	tijdschrift	maand	jaar	pagina

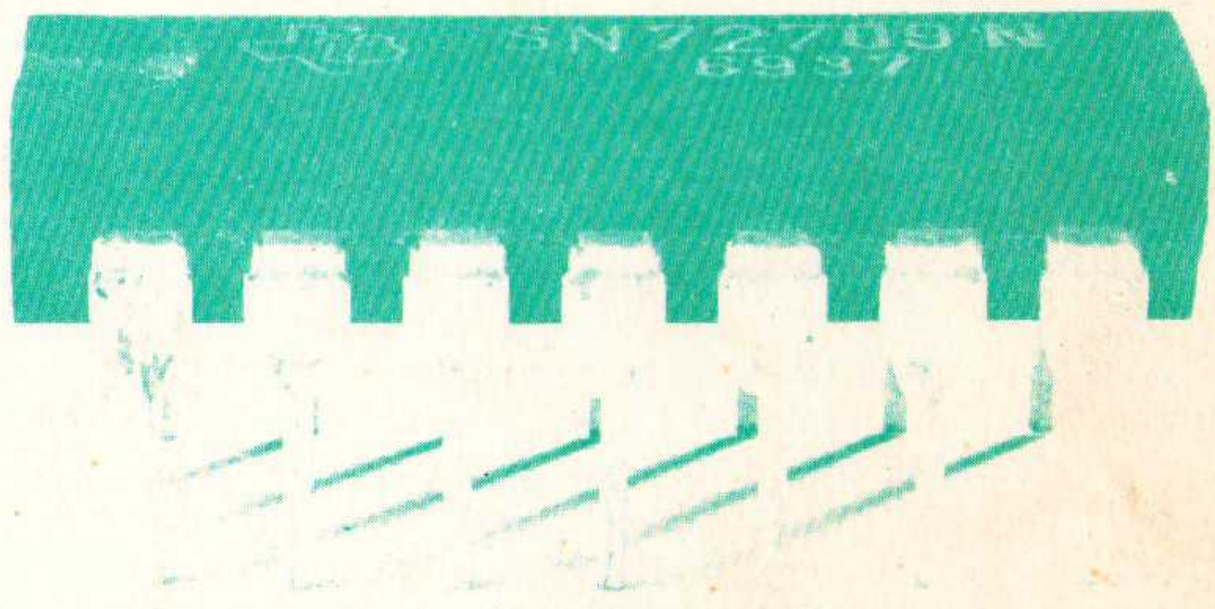
A A N T E K E N I N G E N

N O T E S

Opgenomen schema's met een beknopte omschrijving.

IN DE WERELD VAN KLEINE DINGEN IS VAN DAM GROOT





IN THE WORLD OF SMALL THINGS VAN DAM IS GREAT